FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

DIPLOMA IN ELECTRICAL & ELECTRONIC ENGINEERING

EEE543 – DIGITAL AND ANALOG ELECTRONICS.

FINAL EXAMINATION - TRIMESTER 1 - 2019.

DURATION: 3 HOURS;

TOTAL NO OF PAGES: 9

INSTRUCTIONS TO STUDENTS:

1. You are allowed 10 minutes **EXTRA** as reading time during which you are **NOT** to write.
2. Begin each answer on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each attached sheet.
4. Insert all written foolscap, graph paper, drawing paper, etc. in their correct sequence and secure well.
5. For all sheets of paper on which rough/draft work has been done, cross it through and attach to your answer scripts.
6. Show all workings where necessary
7. Diagrams and graphs can be drawn in pencil.
8. Non- programmable calculators are allowed.
9. **Attempt all questions ie. Sections A B, C, D & E**
10. **Check your work before you leave the room!!**

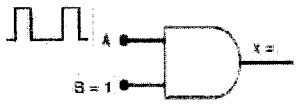
Section A: SHORT ANSWERS (2 marks each) **[20 Marks]**

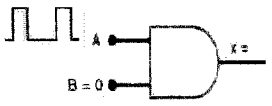
No	Question	Answers
1.	In a JK synchronous Flip Flop, if J = 1 and K = 1, then in the next clock pulse, determine the value of Q?	
2.	Determine the largest decimal number produced in a truth table when using 5 flip flops?	
3.	Explain how to convert a Hexadecimal number to its Octal equivalent?	
4.	Use De-Morgans theorem to simplify the expression $\overline{ABC + DEF}$	
5.	Distinguish two major differences between an analog to a digital system.	
6	Briefly explain the reason why R/2R resistive ladder type is more practical to use than the weighted Resistor type DAC	
7	Sketch switch/relay equivalent circuits for AND and OR gates.	
8	List 2 main difference between TTL and CMOS Logic families	
9.	What is the only input combination that will produce a HIGH at the output of a five-input AND gate?	
10.	What does a negative-going transition "clock" means?	

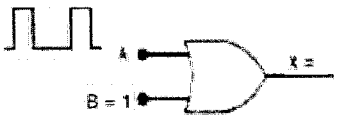
Section B: Number Conversion & Gates [20 marks]

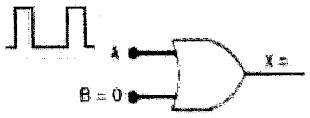
1. Convert the following:
   a) $110101_{GRAYCODE}$ to Binary (2 marks)
   b) 256_8 to BCD (2 marks)
   c) $65A_{16}$ to Binary (2 marks)
   d) 101101_2 to Decimal (2 marks)
   e) Convert 1100101_2 to Gray Code (2 marks)

2. Work out the output x for each gate shown below: **(6 marks)**

a) 

b) 

c) 

d) 

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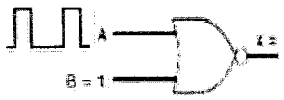
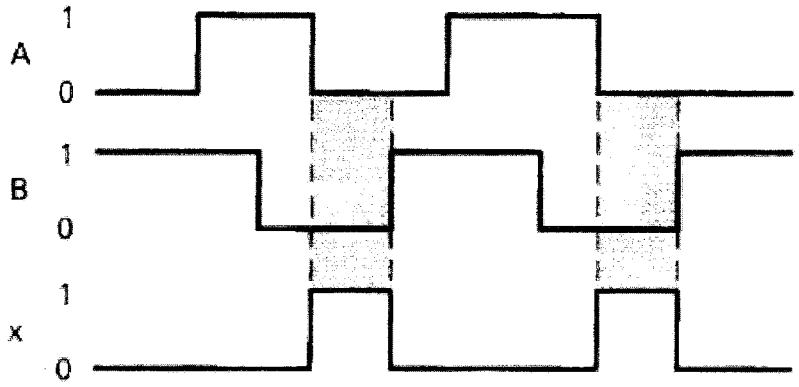
f) 

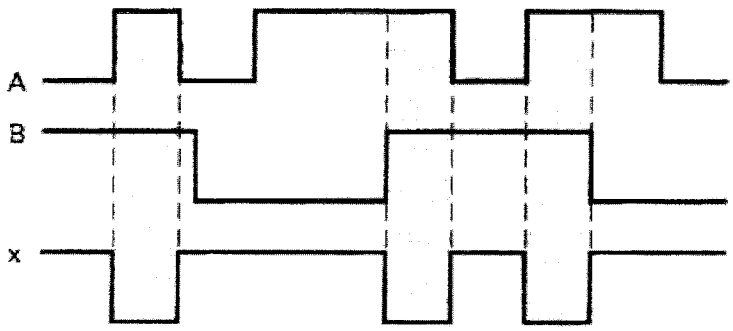
3. Identify the corresponding logic gate of the following waveforms below. A and B are the inputs and X is the output.

a)

(2 marks)



b)



(2 marks)

Section C: Combinational Logic, Boolean & Flip Flops [20marks]

1. Simplify the expression below by using Boolean algebra.

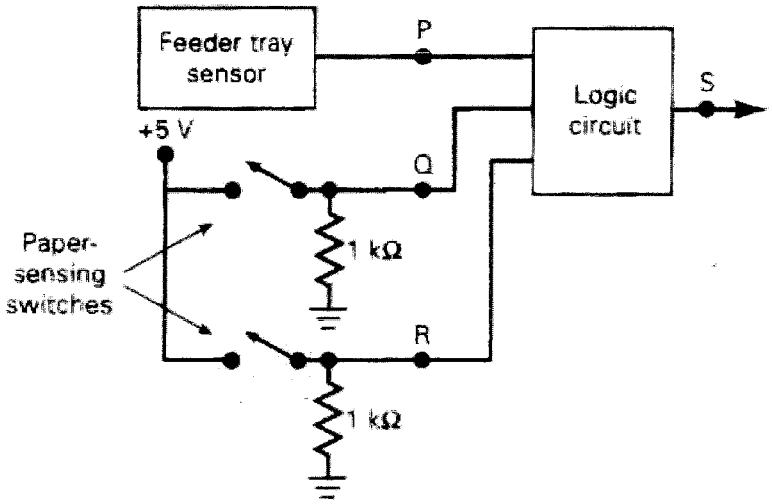
   a) $X = A\overline{B}\,\overline{C} + A\overline{B}C + ABC$ **(2 marks)**

2. Refer to the figure below. In a simple copy machine, a stop signal, S, is to be generated to stop the machine operation and energise an indicator light whenever either of the following conditions exists:

   a) There is no paper in the paper feed tray; OR
   b) The two micro switches in the paper path are activated, indicating a jam in the paper path.

   The presence of paper in the feeder tray is indicated by a HIGH at logic signal P. Each of the micro switch produces a logic signal (Q and R) that goes HIGH whenever paper is passing over the switch to activate it.

   Design the logic circuit to produce a HIGH at output signal S for the stated conditions, and implement it using the 74HC00 CMOS quad two-input NAND chip.



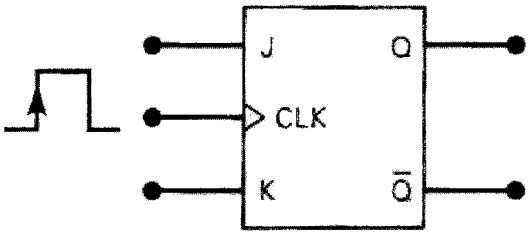
a) **Draw the truth table of the three input combinations.** **(2 marks)**
b) **Determine the Boolean expression from the truth table.** **(2 marks)**
c) Plot the Karnaugh map. (2 marks)
d) **Draw NAND gates only to implement the minimized function** **(2 marks)**

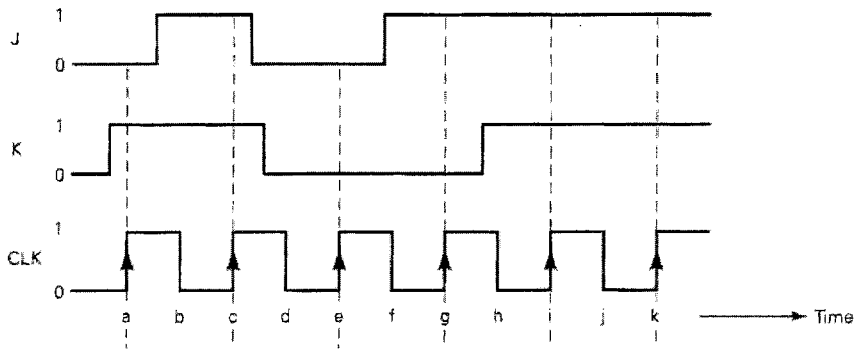
3. Briefly explain the following terms as applied to digital circuits: (4 marks)
   a) Propagation delay
   b) Noise Immunity

4. A clocked JK flip flop is shown below together with the timing diagram of the inputs.

   a) Draw the truth table for a J K Flip flop and determine the output waveform at Q. Assume that Q is initially at a High level; ie a "1" before the first clock.

(6 marks)

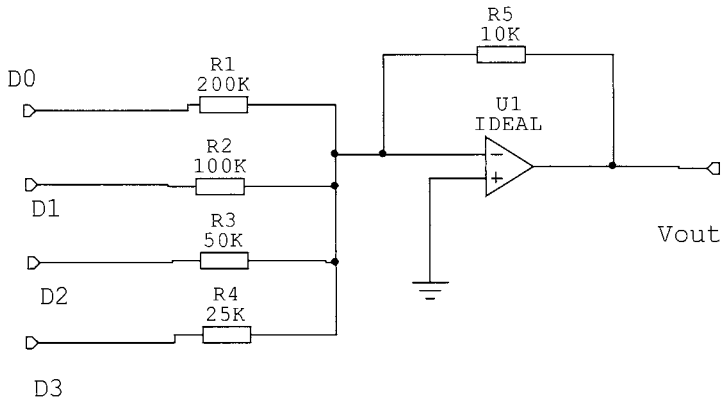




Section D DAC, OPAM Amplifier & BJT & FET [20marks]

1. Figure below shows a four-bit Digital to Analog converter. Logic 1 voltage is 5 V. D3 is the MSB and D0 the LSB.
   Calculate the output voltage (Vout) when the 4-bit digital input word is:

   a) 1001 **(3 marks)**
   b) 1111 **(3 marks)**



   c) What is the one single disadvantage of this type of DAC? **(1 marks)**

2.

   a) Sketch and label the circuit diagrams of an inverting, non-inverting and voltage follower operational amplifier and derive the Gain for each connection? **(6 marks)**

   b). Explain the concept of "virtual ground" in relation to operational amplifier? **(2 marks)**

3

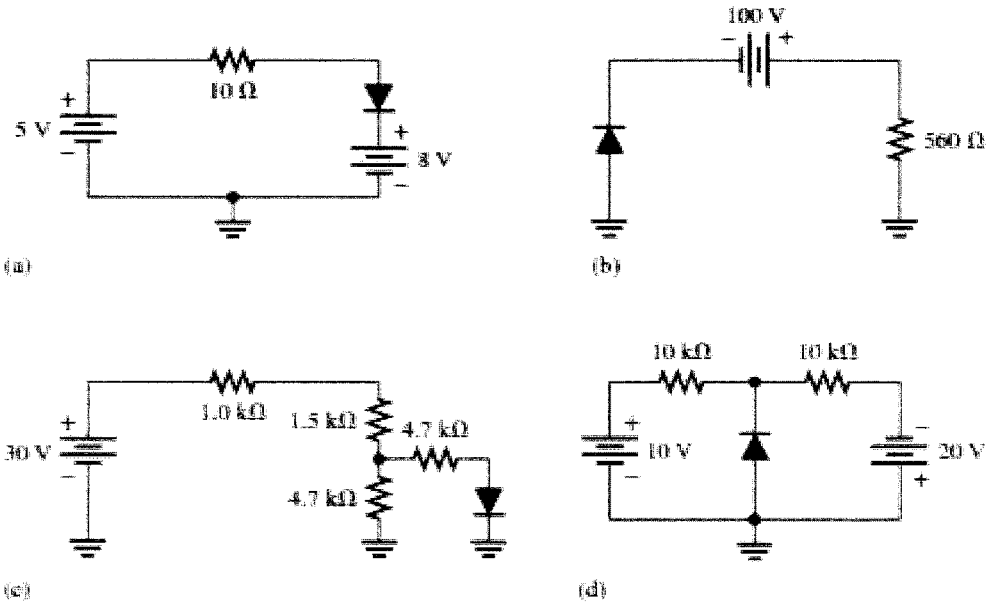
   a). Compare by sketching and labelling an NPN Bipolar transistor symbol and an n-channel JFET symbol and list one applications for each? **(3 marks)**

   b).Determine the dc current gain β_{DC} and the emitter current I_E for a transistor where I_B = 50μA and I_C = 3.65 mA. **(2 marks)**

Section E Rectifiers, Simple Power Supplies & Diodes [20marks]

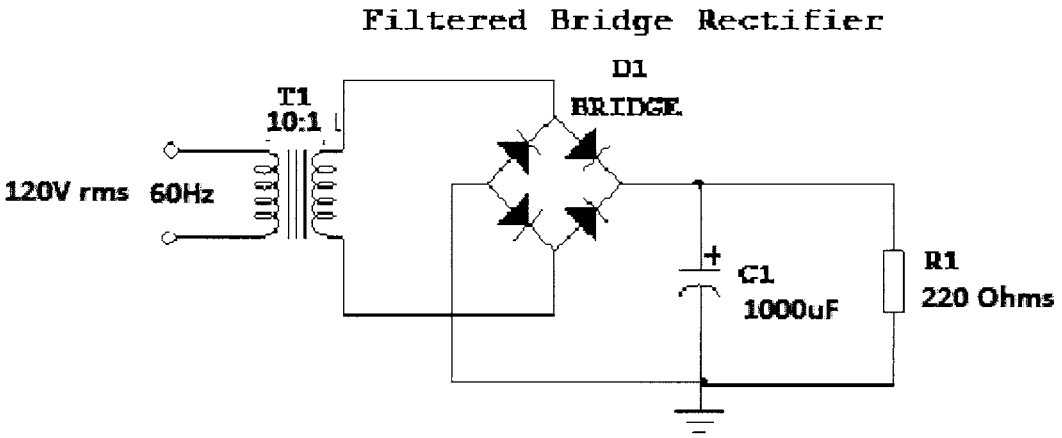
1.

a) Determine whether each silicon diode in figure below is forward –biased or reverse-biased.



(4 marks)

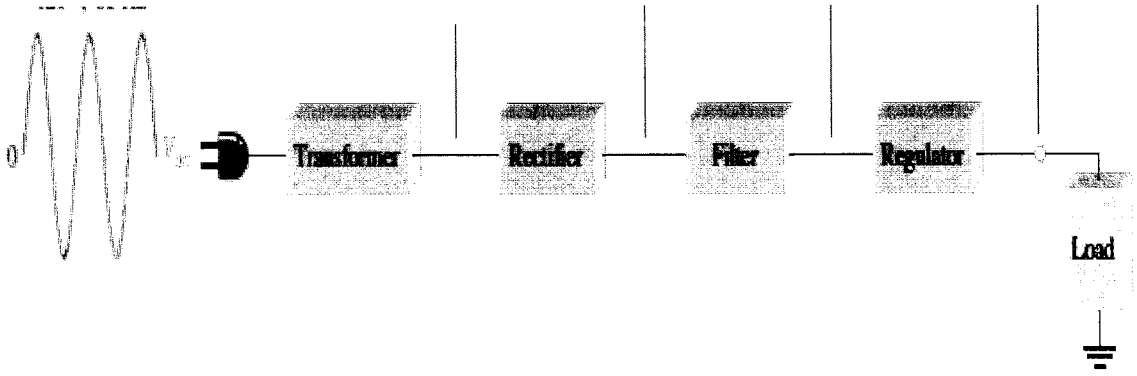
b)



Referring to the Figure above, calculate the following:

i)	The peak primary voltage.	(1 mark)
ii)	The peak secondary voltage	(1 mark)
iii)	The unfiltered peak full wave rectified voltage	(1 mark)
iv)	The peak –to- peak ripple voltage at the output	(2 marks)

C) A basic block diagram of a complete power supply is shown in the figure below. With an AC voltage applied in the primary of the transformer, draw the waveforms at various stages. Assume half-wave rectifier.



(4 marks)

d).Explain why a series resistor is necessary when a diode is operated in forward bias?
(2 marks)

e) State the type and reason for the regulation required for a DC power supply?
(1mark)

f).Sketch a symbol of a zener diode labelling the terminals and discuss its operation and application? **(4 marks)**

----------THE END----------