FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

ADVANCED DIPLOMA IN ENGINEERING (ELECTRICAL & ELECTRONIC)

EEE604 – ELECTRO TECHNOLOGY(ELECTRONIC)

FINAL EXAMINATION – SEMESTER 1, 2019

DAY/DATE: as per ETT TIME: as per ETT

ROOM: TBA

INSTRUCTION TO STUDENT

1. You are allowed 10 minutes extra reading time during which you are **NOT** to write.
2. **Begin each answer (each Question)** on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each answer & attached sheet.
4. Insert all written foolscaps, graph paper etc. in their correct sequence and secure with a string.
5. For all sheets of paper on which rough/draft work has been done, cross it through and you must attach all of them to your answer scripts.
6. Write clearly the number(s) of the question(s) attempted on the top of each sheet.
7. Tables & formula on the Appendix.
8. **SECTION A. - ATTEMPT ALL QUESTIONS**
9. **SECTION B. – CHOOSE ANY TWO(2) QUESTION**

Section – A: - Compulsory Section - Answer all question in this section

Question 1 FET Application

An NMOS inverter in the figure-1 below has the following parameters: $V_{T1} = V_{T2} = 2v$. $\beta_1 = 0.35 \times 10^{-3}$, $\beta_2 = 0.035 \times 10^{-3}$ and $V_{DD} = 12v$.

Determine the ***high*** and *low* output voltage.

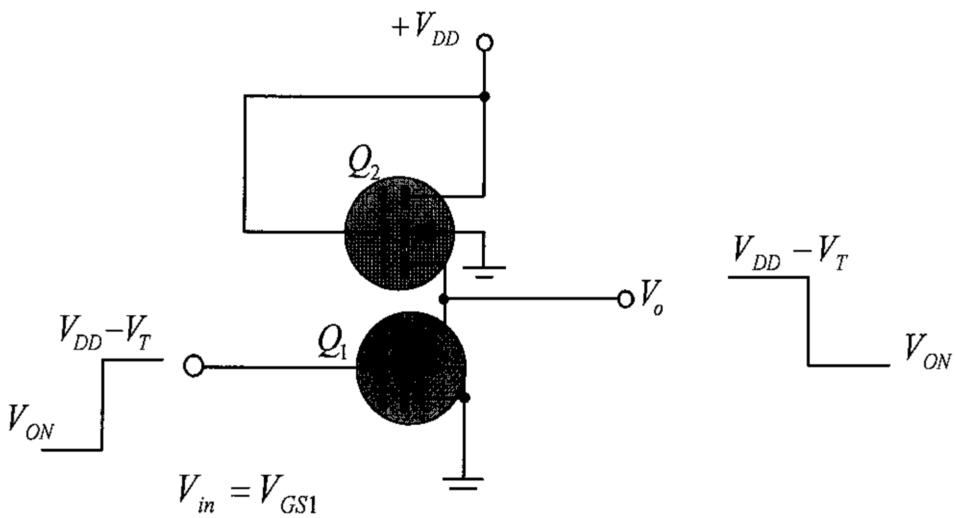

Fig.1 - NMOS Inverter Switch

[Total 20 marks]

Question 2: Class C Power Amplifier

Fig.2 below shows a class C Power Amplifier with base bias voltage of -5v and V_{CC} = 35v. It is determined that a peak input voltage of 7.6V at 1 MHz is required to drive the transistor to its saturation current of 1.6A

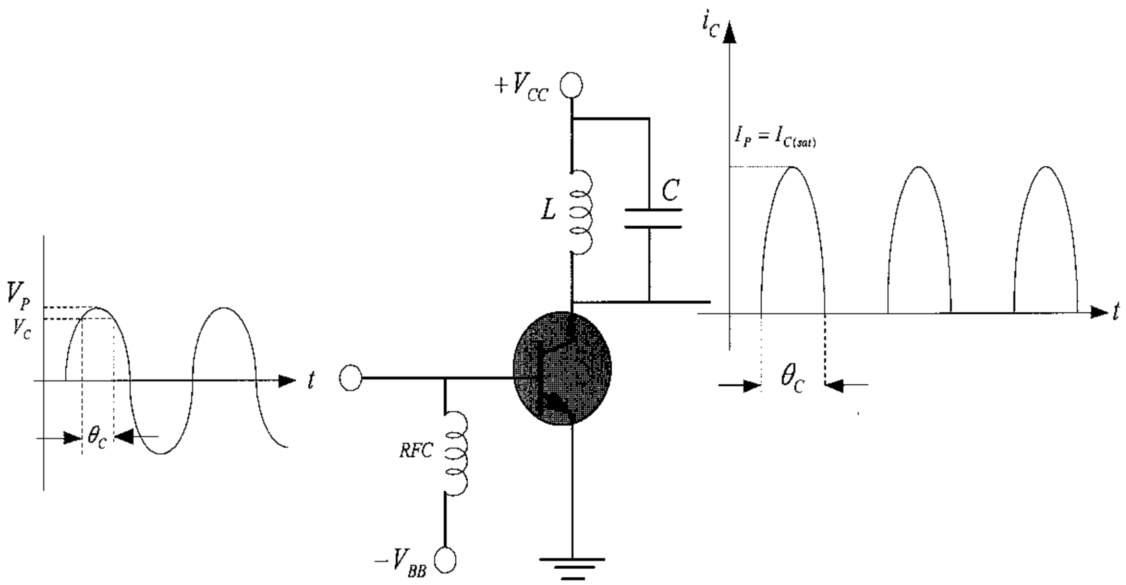

Fig.2 – Class C Power Amplifier

. Determine the following:-

(a). Amplifier's conduction angle. (5 marks)

(b). Amplifier's output power at 1MHz. (5 marks)

(c). Amplifier's efficiency. (4 marks)

(d). If the LC tank circuit having C = 270pF is connected in the collector circuit, find the inductance necessary to tune the amplifier. (6 marks)

[Total 20 marks]

Question 3: Digital System Design & OP amps

(a) Figure 3 below shows a 4-bit synchronous shift register with Q_D output connected back to the DA input via an inverter. Assuming the initial state of the register is 0011.

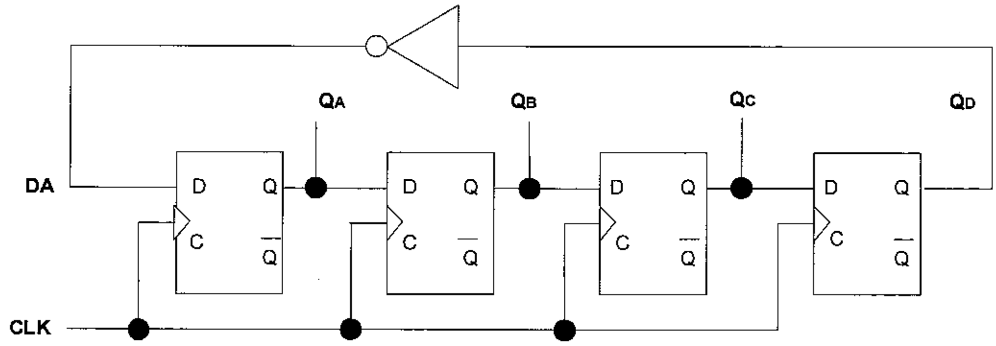

***Figure-3**: 4-bit Shift Register.*

Give a brief account of how the above system works and produce the timing diagram for the output Q_A to Q_D for the next 10 clock pulses, before the output are repeated.

[10 marks]

(b) In a non-inverting circuit in figure-4 below, the input resistance r_{in} of the op amp on its own is 120kΩ and the voltage gain Av of the Op amp is 220,000. [6 marks]

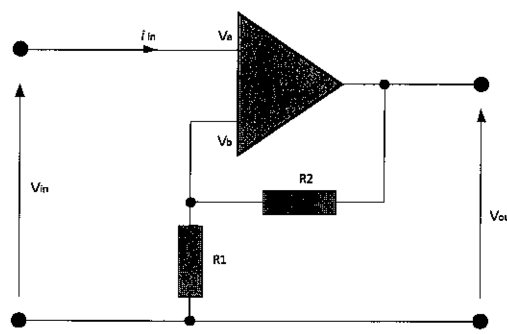

Fig.4 - Non- Inverting Amplifier

Calculate the overall gain G, and the input resistance R_{in} of the circuit above when:-

(i) R_1 = 1KΩ and R_2 = 50KΩ.
(ii) R_1 = 1KΩ, R_2 = 0,
(iii) R_1 = 0KΩ and R_2 = 50KΩ.

(c) Briefly explain the advantages & disadvantages of class-D amplifier system.

[4 marks]

Section B: Optional Section **Answer only 2 question from this section.**

Question - 1 Series Fed Class-A Amplifier

Referring to figure 5 below, an input voltage (V_{in}) in a base current of 10mA peak produces the characteristics shown in fig.4(b) for a series-fed Class A amplifier. Calculate the following: -

(i)	Input Power	(6 marks)
(ii)	Output Power	(6 marks)
(iii)	Efficiency of Amp	(4 marks)
(iv)	Power dissipated by the transistor	(4 marks)

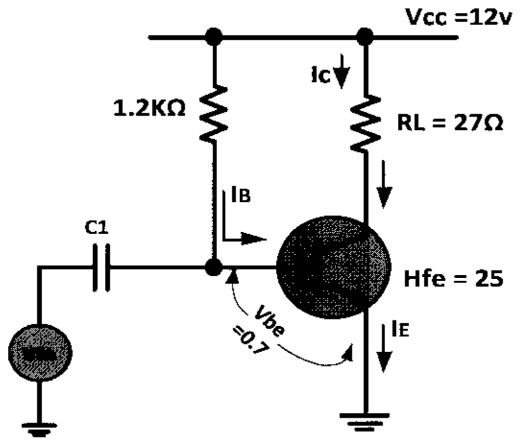

Fig.5a – Series-fed Class A Amplifier

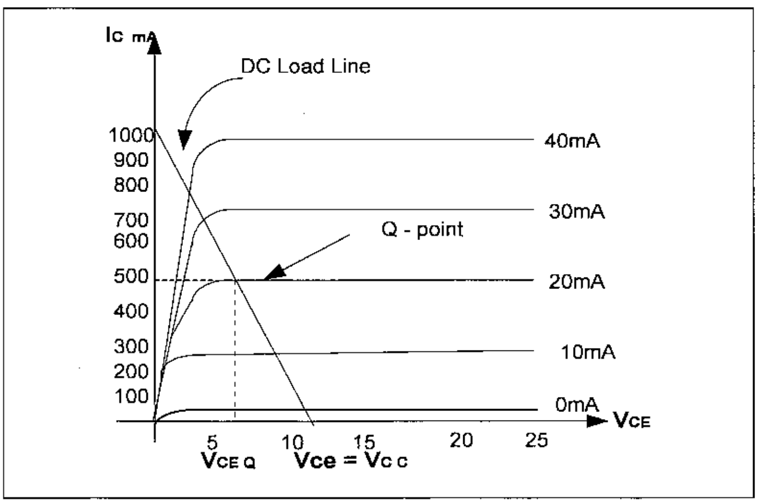

Fig.5b – Series-fed Class A characteristics graph

[20 Marks]

Question – 2: Analysis & Design of Filter circuits

Using the coefficient table attached at the back, design and draw an Active Second Order unity-gain Tschebyscheff Low-pass Filter with a cut-off frequency of 3.5kHz and a 3-dB passband ripple with C1=27nF.

[20 marks]

Question - 3 Analysis & Design of Oscillators circuits

The gain of a certain oscillator system in the fig.6 below as a function of frequency is $A(j\omega) = -16 \times 10^6/j\omega$. A feedback path connected around it has $\beta(j\omega) = 10^3/(2 \times 10^3 + j\omega)^2$.

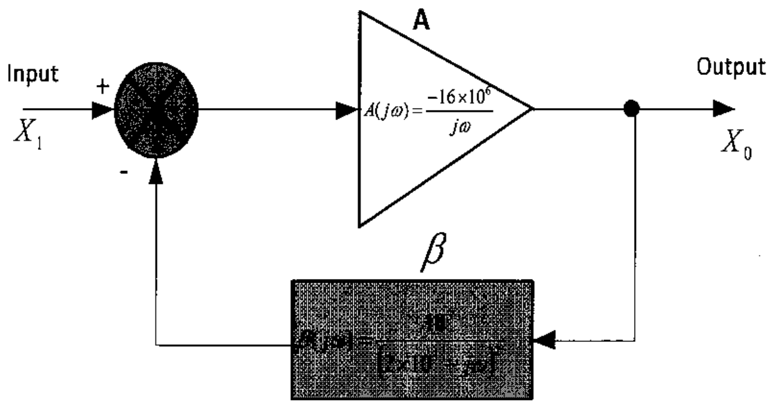

Fig.6 - Oscillator system

(a) Use *Rectangular* form to determine if the system will oscillate or not. (7 marks)

(b) Solve which frequency your design will oscillate. (7 marks)

(c) Name the conditions which oscillators must achieve before it can oscillate. (3 marks)

(d). Write down the difference between the Clapp Oscillator and Colpitts Oscillator. (3 marks)

[20 marks]

Question - 4 Feedback, RC Oscillators & Shift Registers

(a) Identify the golden rule of Negative Feedback system of Op Amp.

[2 marks]

(b) Design & draw an RC Phase shift oscillator using an Amplifier & passive component that oscillates at 200Hz. Assuming that C = 0.68μF, R_I = 47k

[8 marks]

(c) In the address decoding circuit in figure-7 below for a 4 x 8-bit shift register with an address decoder.

(i) Write down the Truth table for the system.
(ii) Write down the address combination which will select the following register B, C, A, D?
(iii) How many output will the three input decoder have?
(iv) Referring to part (iii), write down the truth table

[10 marks]

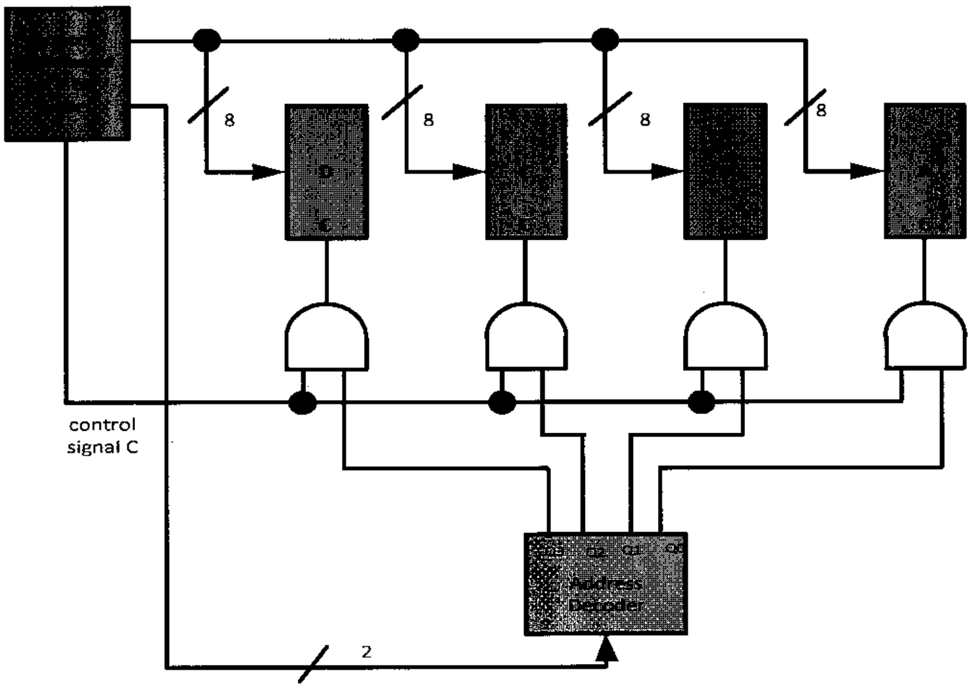

***Figure-7**: 2 Line Address decoder.*

[20 marks]

Question - 5 Characteristics of JFET & BJT Applications

(a) Clearly state all advantages and disadvantages of positive feedback.

[3 marks]

(b) Explain with aid of diagram the effect of increasing V_{DS} in N-Channel JFET, while gate is shorted to source, $V_{GS} = 0$.

[7 marks]

(c) Find the output voltage of the amplifier shown in figure 8 below, assuming that $r_S = 20\Omega$.

[10 marks]

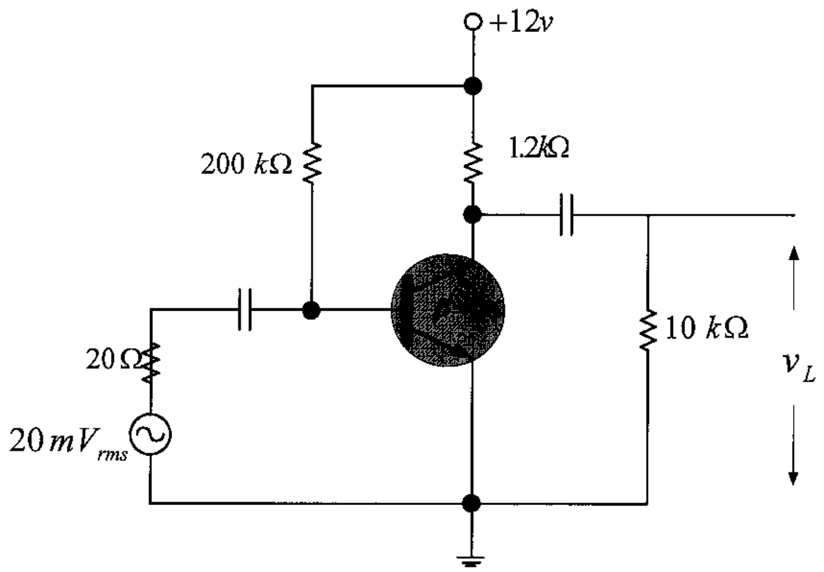

Fig. 8 - Common Emitter BJT amplifier

[Total 20 marks]

-------------THE END ------------

Appendix 1

Formulas

1. $\frac{1}{2}\beta_2\left[(V_{DD}-V_{ON})-V_T\right]^2 = \beta_1\left[(V_{DD}-2V_T)V_{ON}-0.5^2{}_{ON}\right]$

2. $Ai=\frac{hfe}{1+hoe.\ R_L}$ $\qquad$ $A_P=6\left(\frac{D}{\lambda}\right)^2$

3. $C_2=C_1\frac{4b_1}{a_1^{\ 2}}$ $\qquad$ $P_Q=\left(\frac{2}{\pi^2}\times\frac{Vcc^2}{R_L}\right)\Big/2$

4. $K_OK_D=\frac{33.6f_O}{V_C}$ $\qquad$ $X_1=\frac{a_1C_2\pm\sqrt{(a_1C_2)^2-4b_1C_1C_2}}{4\pi f_cC_1C_2}$

5. $X_C=\frac{1}{2\pi fC}$ $\qquad$ $X_L=2\pi fL$ $\qquad$ $P_{i(DC)}=V_{CC}\cdot\left(2/\pi.\ Vcc/R_L\right)$

6. $f=\frac{1}{2\pi\sqrt{6}RC}$ $\qquad$ $I_D=\beta V_{DS}\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)$

7. $Av=\frac{Vo}{Vi}=\left[hre-\frac{hie}{hfe}\left(\frac{1+hoe.R_L{}'}{R_L{}'}\right)\right]^{-1}$ $\qquad$ $I_D=\frac{\beta(V_{GS}-V_T)^2(1+\lambda V_{DS})}{2}$

8. $I_B=\frac{Vcc-0.7v}{R_B}$, $\qquad$ $I_C=h_{FE}.I_B$, $\qquad$ $Vce=Vcc-IcR_L$

9. $I_D=I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$, $\qquad$ $\beta_1\left[(V_{DD}-2V_T)V_{ON}-0.5^2{}_{ON}\right]$

10. $f_H=\pm\frac{8fo}{Vc}$, $\qquad$ $V_{DS}=V_{DD}-I_DR_D$

11. $r_i=\left(-3.54+4.1\theta_C-0.0072\theta_C^2\right)\times10^{-3}$

Appendix 2

Filter Coefficients

SECOND-ORDER	BESSEL	BUTTERWORTH	3-dB TSCHEBYSCHEFF
a_1	1.3617	1.4142	1.065
b_1	0.618	1	1.9305
Q	0.58	0.71	1.3
R_4/R_3	0.268	0.568	0.234

. Second-Order Filter Coefficients

Tschebyscheff Coefficients

n	i	a_i	b_i	$k_i = f_{Ci} / f_C$	Q_i
1	1	1.0000	0.0000	1.000	—
2	1	1.3614	1.3827	1.000	0.86
3	1	1.8636	0.0000	0.537	—
	2	0.0640	1.1931	1.335	1.71
4	1	2.6282	3.4341	0.538	0.71
	2	0.3648	1.1509	1.419	2.94
5	1	2.9235	0.0000	0.342	—
	2	1.3025	2.3534	0.881	1.18
	3	0.2290	1.0833	1.480	4.54
6	1	3.8645	6.9797	0.366	0.68
	2	0.7528	1.8573	1.078	1.81
	3	0.1589	1.0711	1.495	6.51
7	1	4.0211	0.0000	0.249	—
	2	1.8729	4.1795	0.645	1.09
	3	0.4861	1.5676	1.208	2.58
	4	0.1156	1.0443	1.517	8.84
8	1	5.1117	11.960 7	0.276	0.68
	2	1.0639	2.9365	0.844	1.61
	3	0.3439	1.4206	1.284	3.47
	4	0.0885	1.0407	1.521	11.53
9	1	5.1318	0.0000	0.195	—
	2	2.4283	6.6307	0.506	1.06
	3	0.6839	2.2908	0.989	2.21
	4	0.2559	1.3133	1.344	4.48
	5	0.0695	1.0272	1.532	14.58
10	1	6.3648	18.369 5	0.222	0.67
	2	1.3582	4.3453	0.689	1.53
	3	0.4822	1.9440	1.091	2.89
	4	0.1994	1.2520	1.381	5.61
	5	0.0563	1.0263	1.533	17.99