FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE AND TECHNOLOGY
SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

DIPLOMA IN ENGINEERING: ELECTRONICS
(INSTRUMENTATIONS & CONTROL)
(TELECOMMUNICATIONS & NETWORKING)

EED506 DIGITAL ELECTRONICS

FINAL EXAMINATION (SEMESTER 1, 2019)

DURATION OF EXAMINATION = 3 HOURS

DATE/TIME/ROOM – Refer to Exam Timetable

INSTRUCTIONS TO CANDIDATES

1. You are allowed 10 minutes extra time during which you are not to write.
2. Write all your answers in the allocated Answer Booklet.
3. Begin each answer on a fresh new page and use both sides of the sheets.
4. Write your identification number on the top of each attached sheet.
5. Insert all written foolscaps, graph paper, drawing paper, etc in their correct sequence and secure with string provided.
6. For all sheets of paper in which has been done, cross it through and you must attach to your answer script.
7. Write clearly the number(s) of the question(s) attempted on the top of each sheet.
8. Programmable and numbering system calculators are PROHIBITED.
9. All questions are compulsory as each question is 10 marks and equates to 100 marks.

Question 1: Digital logic families – Characteristics, limitations & interfacing (10 marks)

a) Digital electronics evolved so quickly where the innovations and enhancements began from simplicity of technological advancements to where we are today. Basically the ideology started from the diode and ended up in integrated circuits (IC). In digital electronics, ICs are common and are important for the enhancement of the technology. In relations to the above, answer the following:

i. What is propagation delay? (1 mark)

ii. What is power dissipation? (1 mark)

iii. Define fan-in and fan-out. (1 mark)

iv. What is Noise Margin? (1 mark)

v. Define noise immunity. (1 mark)

b) Using Appendix 1, determine the following performance parameters of the 74151 IC:

i. The average power dissipation, $P_{D(avg)}$. (2 marks)

ii. The High-state noise margin, V_{NH}. (1.5 marks)

iii. The Low-state noise margin, V_{NL}. (1.5 marks)

Question 2: Combinational Logic Circuit – Minimisations (10 marks)

Design a multiple-output logic network whose input is a BCD digit and when outputs are defined as follows:

- F1: detects input digits of multiples of 4 that are divisible by 2
- F2: detects numbers greater than or equal to 3
- F3: detects numbers less than 6

a) State the condition and status of this design. (1.5 marks)

b) Implement the truthtable to illustrate the operation of this design. (3.5 marks)

c) Minimise the part b) using karnaugh mapping. (3 marks)

d) Sketch the minimised Boolean Equation logic diagram. (2 marks)

Question 3: MSI Combinational Logic Devices and systems (10 marks)

Use 74151 MUX to build the following system

X_4	X_3	X_2	X_1	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

a) Assume the status (1 mark)

b) Develop its truthtable (5 marks)

c) Sketch the IC showing the realization (4 marks)

Question 4: Sequential Logic Circuits (10 marks)

Design a counter with one control input. When the input is high, the counter should sequence through three states: 10, 01, 11 and repeat. When the input is low the counter should sequence through the same states in the opposite order 11, 01, 10 and repeat.

a) Draw the state diagram and state transition table. (3.5 marks)

b) Implement the counter using D flip flops and whatever gates you like. (4 marks)

c) Is your counter self-starting with the input either high or low? (2.5 marks)

Question 5: Synchronous Counters (10 marks)

Design mod-10 synchronous counter using JK Flip Flops. Check for the lock out condition. If so, how the lock-out condition can be avoided? Draw the neat state diagram and circuit diagram with Flip Flops. (2.5 + 2.5 + 2.5 + 2.5 = 10 marks)

Question 6: Display devices (10 marks)

a) Each segment of a typical 7-segment LED display is rated to operate at 10 mA at 2.7V for normal brightness. Calculate the value of the current-limiting resistor needed to produce approximately 10 mA per segment. (2 marks)

b) Refer to Appendix 2 showing the 7447 datasheet:

i. What is the purpose of $\overline{LT}$? (1 mark)

ii. Using the calculated R_s of part a); sketch the circuit diagram showing the 7447 decoder connected to a common anode 7-segment display. (7 marks)

Question 7: Arithmetic Circuits (10 marks)

Realise a logic diagram using an 8x1 multiplexer (Appendix 1 – 74HC151 MSI IC) by implementing a full adder. The concept of this arithmetic circuit must have three inputs. The process must include:

a) The truthtable. (5 marks)

b) SOP expressions. (2 marks)

c) Logic diagram. (3 marks)

Question 8: Shift register & Decoder (10 marks)

a) Draw the logic diagram of a 4-bit register with four *D flip-flops* and 4x1 multiplexers with mode selection input S_1 and S_0. The register operates according to the following function table: (3 marks)

S_1	S_0	Register Operation
0	0	No change
0	1	Complement for four output
1	0	Clear register to 0 (Synch)
1	1	Load parallel data

b) Implement the function $f(w_1, w_2, w_3) = \sum m(0,1,3,4,6,7)$ by using a 3-to-8 binary decoder and an OR gate. (3 marks)

c) Short answers:

i. The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses? (1 mark)

ii. To operate correctly, starting a ring shift counter requires _____. (1 mark)

iii. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____. (1 mark)

iv. How many clock pulses will be required to completely load serially a 5-bit shift register? (1 mark)

Question 9: DAC and ADC (10 marks)

a) A 5-bit DAC has a current output. For a digital input of 10100, an output current of 10 mA is produced. What will I_{OUT} be for a digital input of 11101? (3.5 marks)

b) Assume the following values for the ADC clock frequency = 1MHz; V_T = 0.1 mV; DAC has full scale output = 10.23 V and a 10-bit input. Determine the following values:

i. The digital equivalent obtained for V_A = 3.728 V. (4 marks)

ii. The conversion time. (0.5 marks)

iii. The resolution of this converter. (2 marks)

Question 10: Programmable Logic Devices Architecture (10 marks)

a) List any two types of programmable logic devices. (2 marks)

b) Using Programmable Logic Array, implement the following functions:

- $F_1 = ABC$
- $F_2 = A + B + C$
- $F_3 = \bar{A}\bar{B}\bar{C}$
- $F_4 = \bar{A} + \bar{B} + \bar{C}$
- $F_5 = A\ xor\ B\ xor\ C$
- $F_6 = \overline{(A\ xnor\ B\ xnor\ C)}$ (8 marks)

----------END----------

Appendix 1 74151 MSI IC datasheet

74HC151; 74HCT151

8-input multiplexer

Rev. 6 — 28 December 2015 **Product data sheet**

1. General description

The 74HC151; 74HCT151 are 8-bit multiplexer with eight binary inputs (I0 to I7), three select inputs (S0 to S2) and an enable input ($\overline{E}$). One of the eight binary inputs is selected by the select inputs and routed to the complementary outputs (Y and $\overline{Y}$). A HIGH on $\overline{E}$ forces the output Y LOW and output $\overline{Y}$ HIGH. Inputs also include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Specified in compliance with JEDEC standard no. 7A
- Input levels:
  - For 74HC151: CMOS level
  - For 74HCT151: TTL level
- Low-power dissipation
- Non-inverting data path
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC151D 74HCT151D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC151DB 74HCT151DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC151PW 74HCT151PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

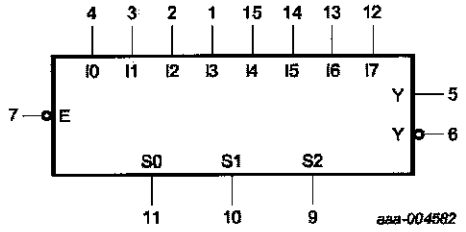


Fig 1. Logic symbol

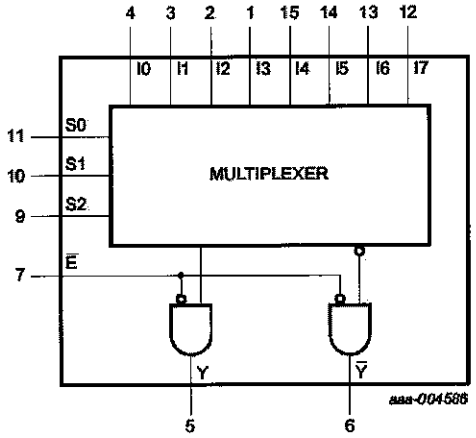


Fig 2. Functional diagram

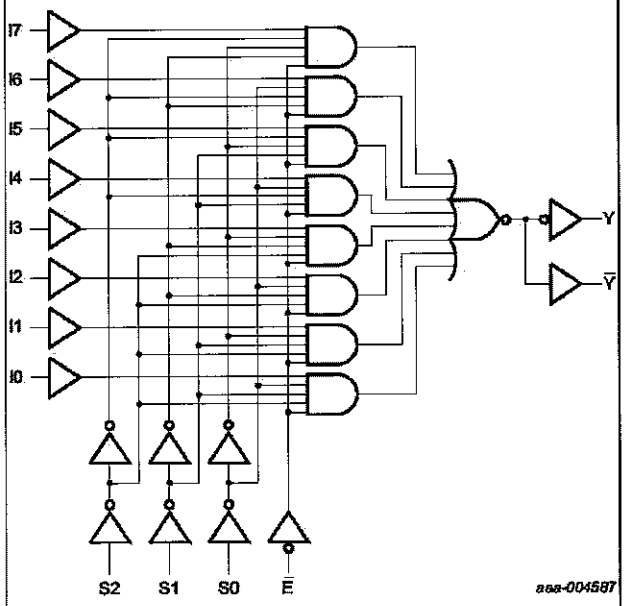


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

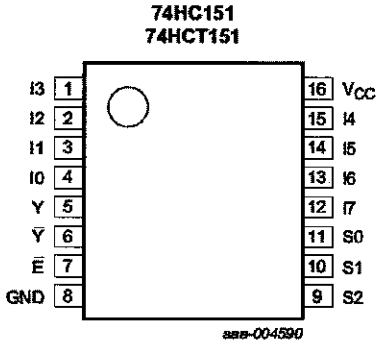


Fig 4. Pin configuration SO16 and (T)SSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
I0 to I7	4, 3, 2, 1, 15, 14, 13, 12	data inputs
Y	5	multiplexer output
$\overline{Y}$	6	complementary multiplexer output
$\overline{E}$	7	enable input (active LOW)
GND	8	ground (0 V)
S0, S1, S2	11, 10, 9	common data select inputs
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Input												Output	
E	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	Y	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C

Table 4. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C				
		SO16 package	[1]	-	500	mW
		(T)SSOP16 package	[2]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[2] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC151			74HCT151			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		T_{amb} = −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC151										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		T_{amb} = −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT151										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		per input pin; In inputs	-	45	162	-	203	-	221	μA
		per input pin; $\overline{E}$ input	-	30	108	-	135	-	147	μA
		per input pin; Sn input	-	150	540	-	675	-	735	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Appendix 2: 7447 MSI IS Datasheet

FAIRCHILD SEMICONDUCTOR™

September 1986
Revised July 2001

DM7446A, DM7447A
BCD to 7-Segment Decoders/Drivers

General Description

The DM7446A and DM7447A feature active-LOW outputs designed for driving common-anode LEDs or incandescent indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

All of the circuits incorporate automatic leading and/or trailing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a HIGH logic level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing) or to inhibit the outputs.

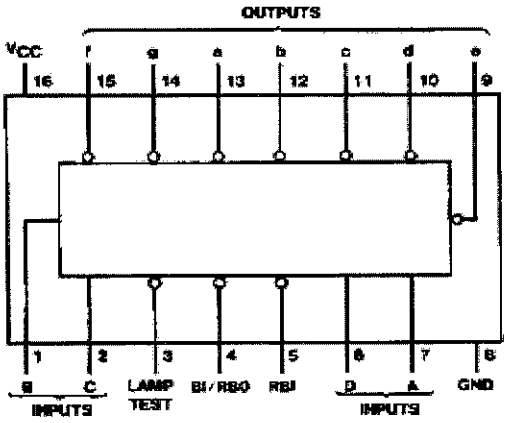
Features

- All circuit types feature lamp intensity modulation capability
- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

Ordering Code:

Order Number	Package Number	Package Description
DM7446AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
DM7447AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



 DS006518 www.fairchildsemi.com

Function Table

Decimal or Function	Inputs						BI/RBO (Note 1)	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	(Note 2)
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 3)
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 4)
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 5)

H = HIGH level, L = LOW level, X = Don't Care

Note 1: BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

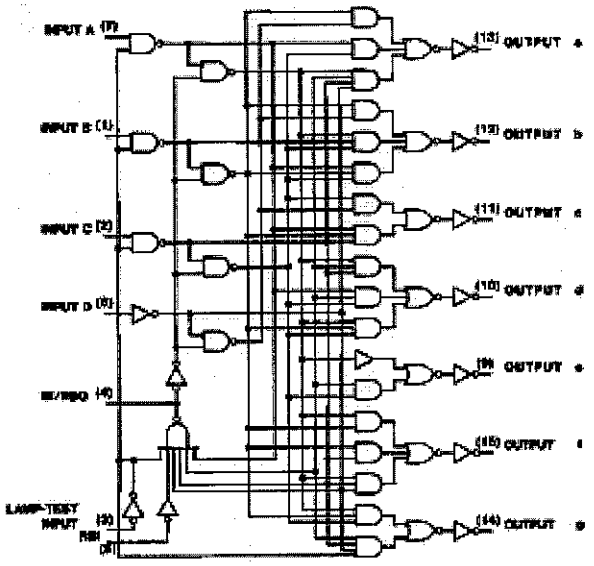
Note 2: The blanking input (BI) must be OPEN or held at a HIGH logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be OPEN or HIGH if blanking of a decimal zero is not desired.

Note 3: When a LOW logic level is applied directly to the blanking input (BI), all segment outputs are HIGH regardless of the level of any other input.

Note 4: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a LOW level with the lamp-test input HIGH, all segment outputs go H and the ripple-blanking output (RBO) goes to a LOW level (response condition).

Note 5: When the blanking input/ripple-blanking output (BI/RBO) is OPEN or held HIGH and a LOW is applied to the lamp-test input, all segment outputs are L.

Logic Diagram



Absolute Maximum Ratings(Note 6)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 6: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
DM7446A					
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
V_{OH}	HIGH Level Output Voltage (a thru g)			30	V
I_{OH}	HIGH Level Output Current (BI/RBO)			−0.2	μA
I_{OL}	LOW Level Output Current (a thru g)			40	mA
I_{OL}	LOW Level Output Current (BI/RBO)			8	mA
T_A	Free Air Operating Temperature	0		70	°C
DM7447A					
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
V_{OH}	HIGH Level Output Voltage (a thru g)			15	V
I_{OH}	HIGH Level Output Current (BI/RBO)			−0.2	μA
I_{OL}	LOW Level Output Current (a thru g)			40	mA
I_{OL}	LOW Level Output Current (BI/RBO)			8	mA
T_A	Free Air Operating Temperature	0		70	°C

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DM7446A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 7)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage (BI/RBO)	V_{CC} = Min I_{OH} = Max		2.4	3.7		V
I_{OEX}	HIGH Level Output Current (a thru g)	V_{CC} = Max, V_O = 30V V_{IL} = Max, V_{IH} = Min				250	µA
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V (Except BI/RBO)				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V (Except BI/RBO)				40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 8)			60	103	mA

Note 7: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 8: I_{CC} is measured with all outputs OPEN and all inputs at 4.5V.

DM7446A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF R_L = 120Ω		100	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			100	ns

DM7447A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 9)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage (BI/RBO)	V_{CC} = Min I_{OH} = Max		2.4	3.7		V
I_{CEX}	HIGH Level Output Current (a thru g)	V_{CC} = Max, V_O = 15V V_IL = Max, V_{IH} = Min				250	µA
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 10)			60	103	mA

Note 9: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 10: I_{CC} is measured with all outputs OPEN and all inputs at 4.5V.

DM7447A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF R_L = 120Ω		100	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			100	ns