FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE AND TECHNOLOGY
SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

DIPLOMA IN ENGINEERING: ELECTRICAL

EED503 DIGITAL & ANALOGUE ELECTRONICS

FINAL EXAMINATION (SEMESTER 1, 2019)

DURATION OF EXAMINATION = 3 HOURS

DATE/TIME/ROOM – Refer to Exam Timetable

INSTRUCTIONS TO CANDIDATES

1. You are allowed 10 minutes extra time during which you are not to write.
2. Write all your answers in the allocated Answer Booklet.
3. Begin each answer on a fresh new page and use both sides of the sheets.
4. Write your identification number on the top of each attached sheet.
5. Insert all written foolscaps, graph paper, drawing paper, etc in their correct sequence and secure with string provided.
6. For all sheets of paper in which has been done, cross it through and you must attach to your answer script.
7. Write clearly the number(s) of the question(s) attempted on the top of each sheet.
8. Programmable and numbering system calculators are PROHIBITED.
9. All questions are compulsory as each question is 10 marks and equates to 100 marks.

Question 1: Digital: basic principles, logic functions and gates

(10 marks)

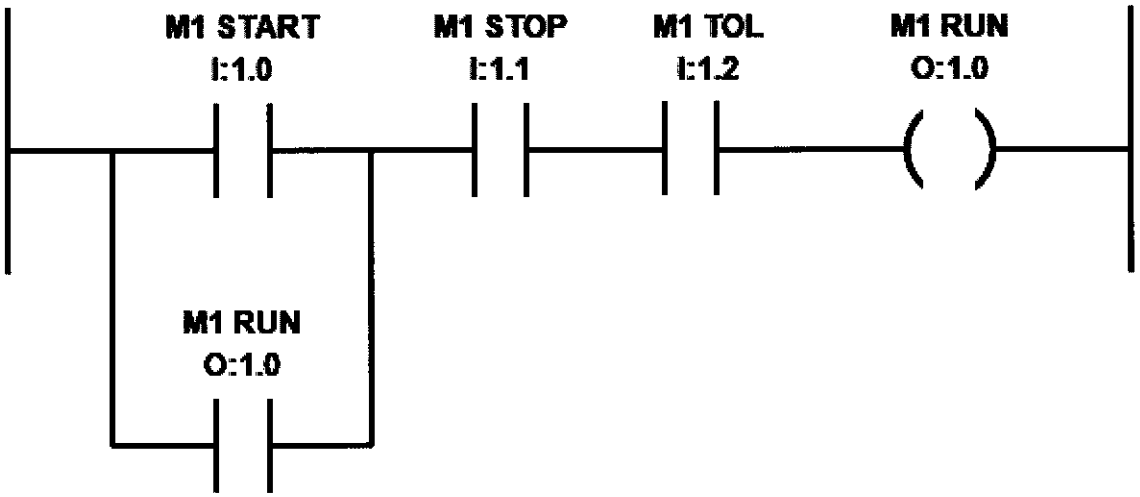
a) Discuss one difference between a digital quantity and an analog quantity in terms of an application in electrical engineering. (2 marks)

b) A task was assigned to you by your supervisor at work to decode the following numbering systems containing hexadecimal, binary, octal and decimal numbering sequence. Determine the following to determine the equivalent by showing the working: (Use the shortest method to resolve)

$14B_{16} + 11101101_2 + 136_8 =$ _____$_{10} =$ _____$_{16}$

(2+2=4 marks)

c) Decode the given ladder logic by determining the Boolean Equation representation of it.

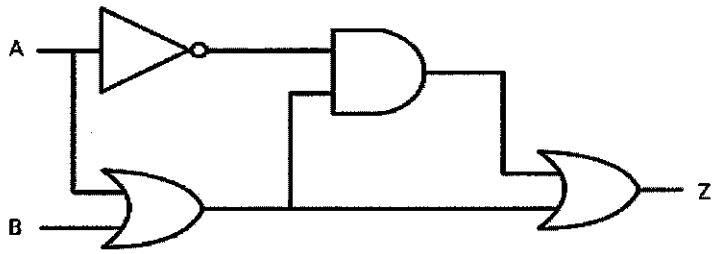


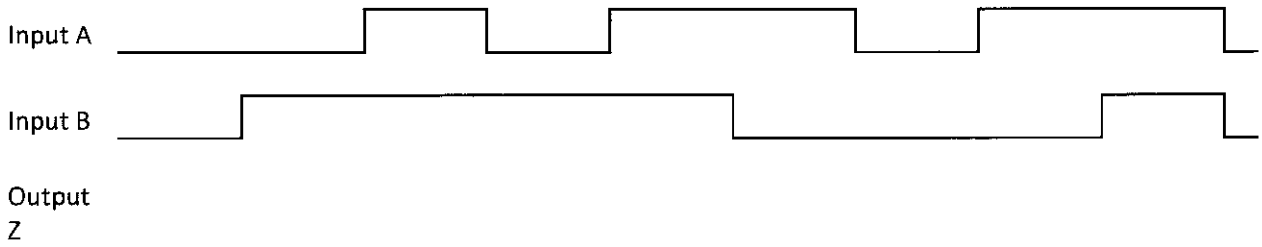
Represent the literals as:

- A – I:1.0
- B – I: 1.1
- C – I: 1.2
- X – O:1.0

(2 marks)

d) From a given diagnostic test on a digital equipment, you as the qualified electrician noticed the given integrated circuit setup and your supervisor knowing you had done a unit in digital & analogue electronics had asked you to analyse the given logic diagram by determining the timing diagram of the output of the logic diagram. (Use Appendix 1 to complete the timing diagram.) (2 marks)





Question 2: Digital: Boolean algebra (10 marks)

a) Using the Boolean Theorems and Laws in Appendix 2, compute a minimised Boolean Equation for the following: (Show all working with associated theorems and laws used)

i. $Z = (A + \bar{B} + \bar{C})(A + \bar{B}C)$ (1.5 marks)

ii. $X = \overline{(\bar{A} + C)(B + \bar{D})}$ (1.5 marks)

b) Convert the following Boolean Equations using universal gates and sketch the equivalence:

i. $Y = \overline{\overline{(\bar{A} + \bar{B})} + \overline{(\bar{C} + \bar{D})}}$ using NAND gates. (3 marks)

ii. $X = \overline{\overline{(A\bar{B}.\overline{BCD})}.\overline{(\bar{C} + \bar{D})}}$ Using NOR gates. (4 marks)

Question 3: Digital: Combinational logic circuits (10 marks)

An electrical cabling manufacturing plant needs to have a horn sound to signal quitting time. The horn should be activated when all of the following conditions is met:

- It's after 5 o'clock and all machines are shut down.
- If there is a machine breakdown time.
- Its Friday, the production run for the day is complete, and all machines are shut down.

Design a logic circuit that will control the horn on the status that four input literals are to represent the various conditions.

a) State the condition and status of this design. (1 mark)
b) Implement the truthtable to illustrate the operation of this design. (2 marks)
c) Derive the Boolean Equation in relations to part a). (1 mark)
d) Minimise the part c) using karnaugh mapping. (3 marks)
e) Sketch the minimised Boolean Equation logic diagram. (2 marks)
f) Proof the minimised Boolean equation in relations to the design. (1 mark)

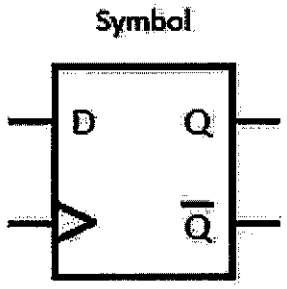
Question 4: Digital: Flip flops and sequential circuits (10 marks)

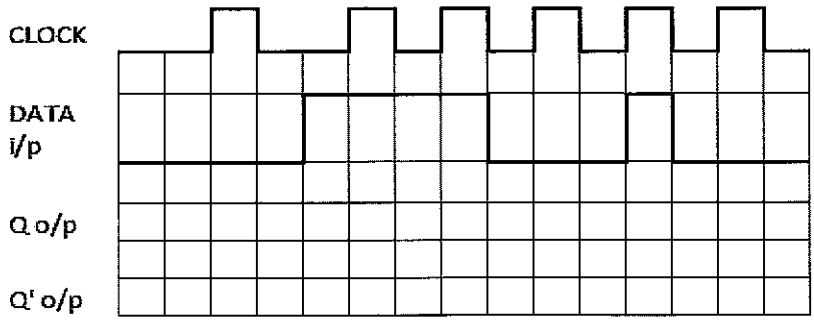
a) Design a MOD 10 asynchronous up-counter using JK flipflops with a negative edge trigger. Show the analysis using the timing diagram and sketch the state diagram. (Use the JK flipflop datasheet in appendix 5 to assist you)

(3 + 2 + 1 = 6 marks)

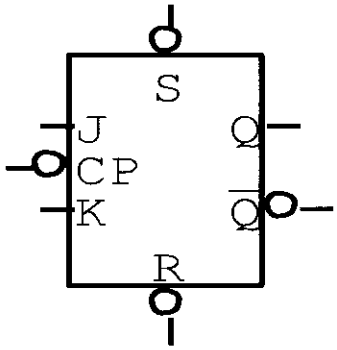
b) Determine the timing diagram by using Appendix 3 and attaching it to your answer booklet:

(2 marks)



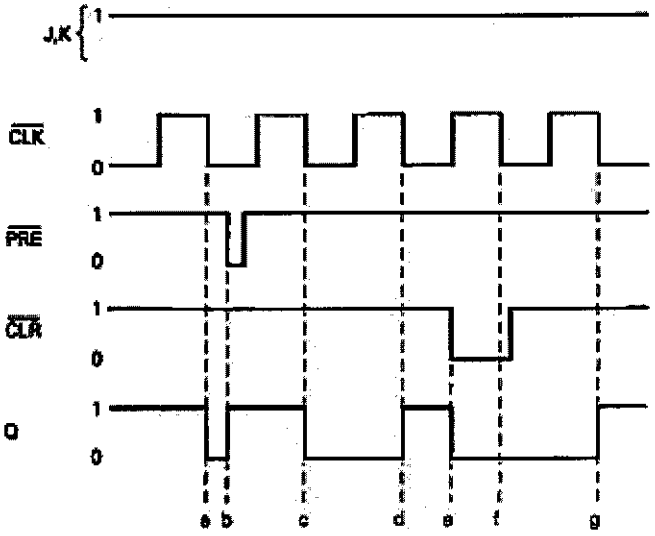


c) Discuss the operations of the given setup shown below: (2 marks)



Note:

- $\overline{PRE} = S$
- $\overline{CLR} = R$
- $\overline{CLK} = CP$ (0 *to* 1)
- J & K *inputs* $= +5V$



Question 5: Digital: Logic families (10 marks)

a) Sketch a DIP IC package for a SN7400 and label the pin numbers. Show the indicator to identify pin 1. (2 marks)

b) Using Appendix 5, determine the following performance parameters of the 7432 IC:

i. The average power dissipation, $P_{D(avg)}$. (2 marks)

ii. The High-state noise margin, V_{NH}. (1.5 marks)

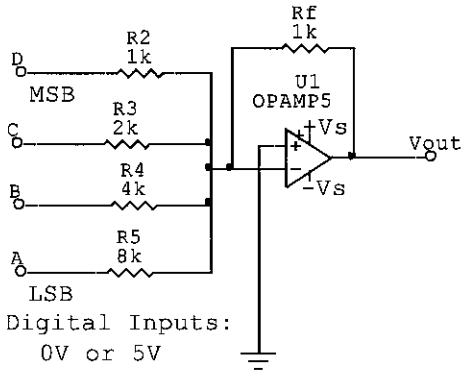
iii. The Low-state noise margin, V_{NL}. (1.5 marks)

c) What does the IC inscription "DM74LS32" mean? (3 marks)

Question 6: Digital: Digital-to-analog conversion, analog-to-digital conversion (10 marks)

a) Draw the block diagram of system having the ADC and DAC along with a transducer and an actuator. Discuss the stages of this block diagram. (2.5 + 2.5 = 5 marks)

b) Determine the DAC voltage output of the given circuit. (5 marks)



SI unit OF Resistors = ohms

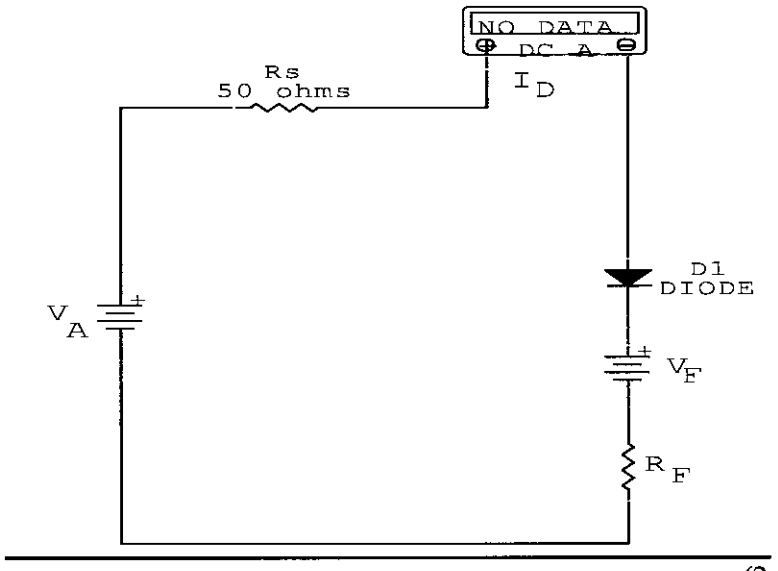
Question 7: Digital: Display devices (10 marks)

a) Sketch the seven-segment common anode display and label the segments. Draw its schematic diagram. (3.5 + 3.5 = 7 marks)

b) Using the seven-segment common cathode datasheet in Appendix 4, determine the limiting resistor value if the supply voltage is 5V if green one is used. (3 marks)

Question 8: Analogue: Analog basics: rectifiers & single phase rectifier configuration (10 marks)

a) Use Kirchhoff's Voltage Law to determine the value of I_D if V_A of the given circuit is 5V. (Note the diode used is made from germanium)



(2 marks)

b) Distinguish by discussing the difference of a forward biased diode operation to a reverse biased diode operation. Draw and label the diagram to show this operation.

(2 + 2 = 4 marks)

c) Draw a schematic diagram of a half-wave rectifier and sketch its waveforms. (4 marks)

Question 9: Analogue: Simple power supplies (10 marks)

As a qualified electrician after undergoing this unit, you were given a task to construct a simple power supplied which will be used to power up a 5V stabilized source equipment. Your tasks are as follows:

a) Draw and label the block diagram. Describe the stages of this block diagram with the required waveforms. (2.5 + 2.5 = 5 marks)

b) Design the 5V power supply schematic diagram and list all materials required for this construction. (Include the hypothesis and assumptions. Show all workings and analysis)

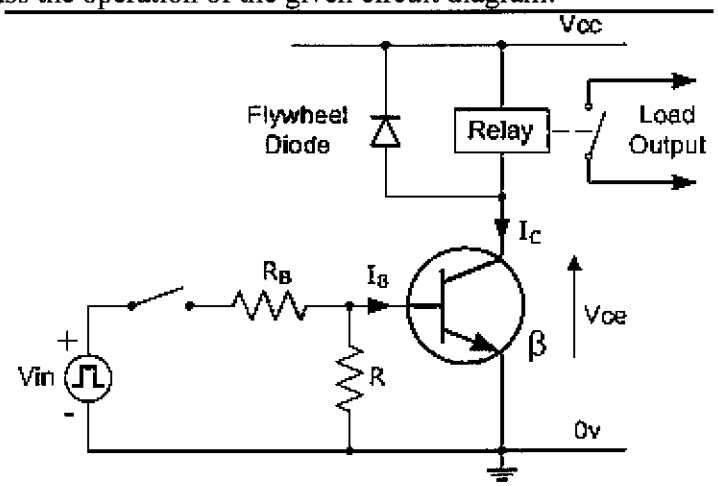
(5 marks)

Question 10: **Analogue: Amplifying principles, IC amplifying devices, discrete amplifying devices and circuits (10 marks)**

a) List ideal performance parameters of an op-amp. (2 marks)

b) An NPN transistor has a DC base bias voltage, V_b of 10V and an input base resistor, R_b of 100 kΩ. What will be the value of the base current, I_b; into the transistor. (The transistor is made of silicon) (1.5 marks)

c) Discuss the operation of the given circuit diagram: (3.5 marks)

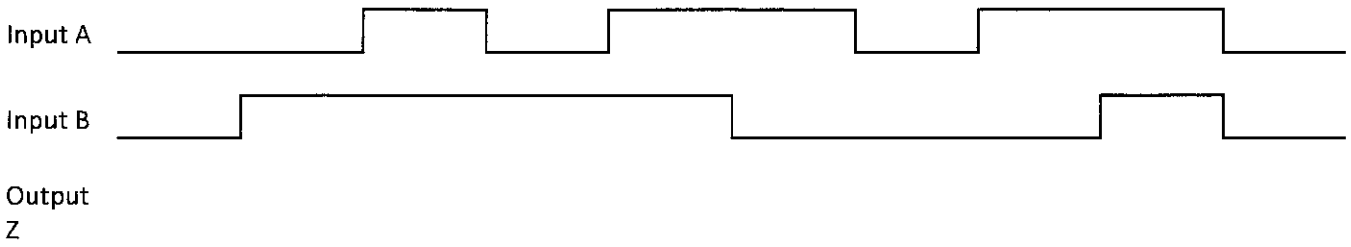


d) Briefly describe the specification of a phototransistor. (1.5 marks)

e) List the two types of field effect transistors (FET) and briefly elaborate the differences. (1.5 marks)

----------END----------

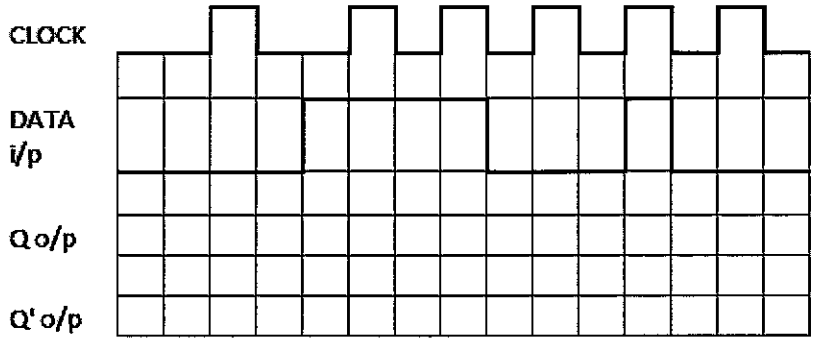
Appendix 1 **(Attached to the answer sheet)** **STUDENT'S ID #:.....**



Appendix 2: Boolean Theorems and Laws

Law/Theorem	Law of Addition	Law of Multiplication
Identity Law	$x + 0 = x$	$x \cdot 1 = x$
Complement Law	$x + x' = 1$	$x \cdot x' = 0$
Idempotent Law	$x + x = x$	$x \cdot x = x$
Dominant Law	$x + 1 = 1$	$x \cdot 0 = 0$
Involution Law	$(x')' = x$	
Commutative Law	$x + y = y + x$	$x \cdot y = y \cdot x$
Associative Law	$x+(y+z) = (x+y)+z$	$x \cdot (y \cdot z) = (x \cdot y) \cdot z$
Distributive Law	$x \cdot (y+z) = x \cdot y+x \cdot z$	$x+y \cdot z = (x+y) \cdot (x+z)$
Demorgan's Law	$(x+y)' = x' \cdot y'$	$(x \cdot y)' = x' + y'$
Absorption Law	$x + (x \cdot y) = x$	$x \cdot (x + y) = x$

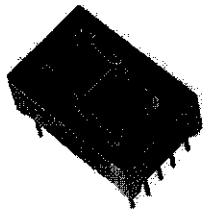
Appendix 3: **STUDENT'S ID #:.....**



Appendix 4

Common Cathode 0.36 Inch (9.14 mm)

Product Features
(1) 0.36 inch (9.14 mm) Digit Height
(2) Low current operation
(3) Excellent colour & font characteristics
(4) Colours: White, blue, red, yellow and green
(5) Gray or black coloured background
(6) Common cathode
(7) RoHs Compliant Part



Absolute Maximum Rating (Ta = 25°C)

Parameter	RED	AMBER	GREEN	BLUE	WHITE	UNITS
DC Forward current per segment	30	30	25	30	20	mA
Peak current per segment[1]	70	50	50	25	25	mA
Avg. forward current per segment	30	30	25	25	25	mA
Derating linear from 25°C/segment	0.3					mA/°C
Reverse voltage[2]	3					V
Operating temperature	-25 to +85					°C
Storage temperature	-30 to +85					°C

(1) Pulse conditions of 1/10 duty and 0.1msec width, for long operating life, max. of 20mA recommended.
(2) Reverse biasing of the dot matrix is not recommend, will cause damage to the LEDs

Electro-optical Characteristics (Ta = 25°C)

Part number	Dice material (colour)	Peak wavelength (nm)	Max reverse current/segment (uA)	V_F (V) Typical	V_F (V) Maximum	Luminous intensity/segment average (I_F = 10mA)
LED53632AUR1C	AlGaAs Red	660	10	1.8	2.3	8,000 ucd
LED53632TB1C	InGaN Blue	468	10	3.3	4.0	20,000 ucd
LED53632YG1C	GaP Green	568	10	1.9	2.3	8,000 ucd
LED53632UY1C	AlInGaP Amber	590	10	1.8	2.3	12,000 ucd
LED53612TW1C	InGan White	5,500K	10	3.3	4.0	20,000 ucd

Appendix 5

Note that on the next page, you will the datasheet of the ICs 7476 and 7432

FAIRCHILD SEMICONDUCTOR™

March 1998

DM7476
Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

General Description

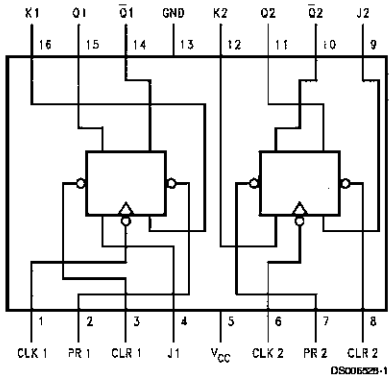
This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be allowed to change while the clock is high. The data is transfered to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (5476) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 5476DMQB, 5476FMQB, DM5476J, DM5476W or DM7476N
See Package Number J16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transfered to the outputs on the falling edge of the clock pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		DM5476			DM7476			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 8)		0		15	0		15	MHz
t_W	Pulse Width (Note 8)	Clock High	20			20			ns
		Clock Low	47			47			
		Preset Low	25			25			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Notes 3, 8)		0↑			0↑			ns
t_H	Input Hold Time (Notes 3, 8)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
			Preset			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V (Note 7)	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
			Preset			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			18	34	mA

Note 3: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference (↑) for rising edge, (↓) for falling edge.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time.

Note 6: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Note 7: Clear is measured with preset high and preset is measured with clear high.

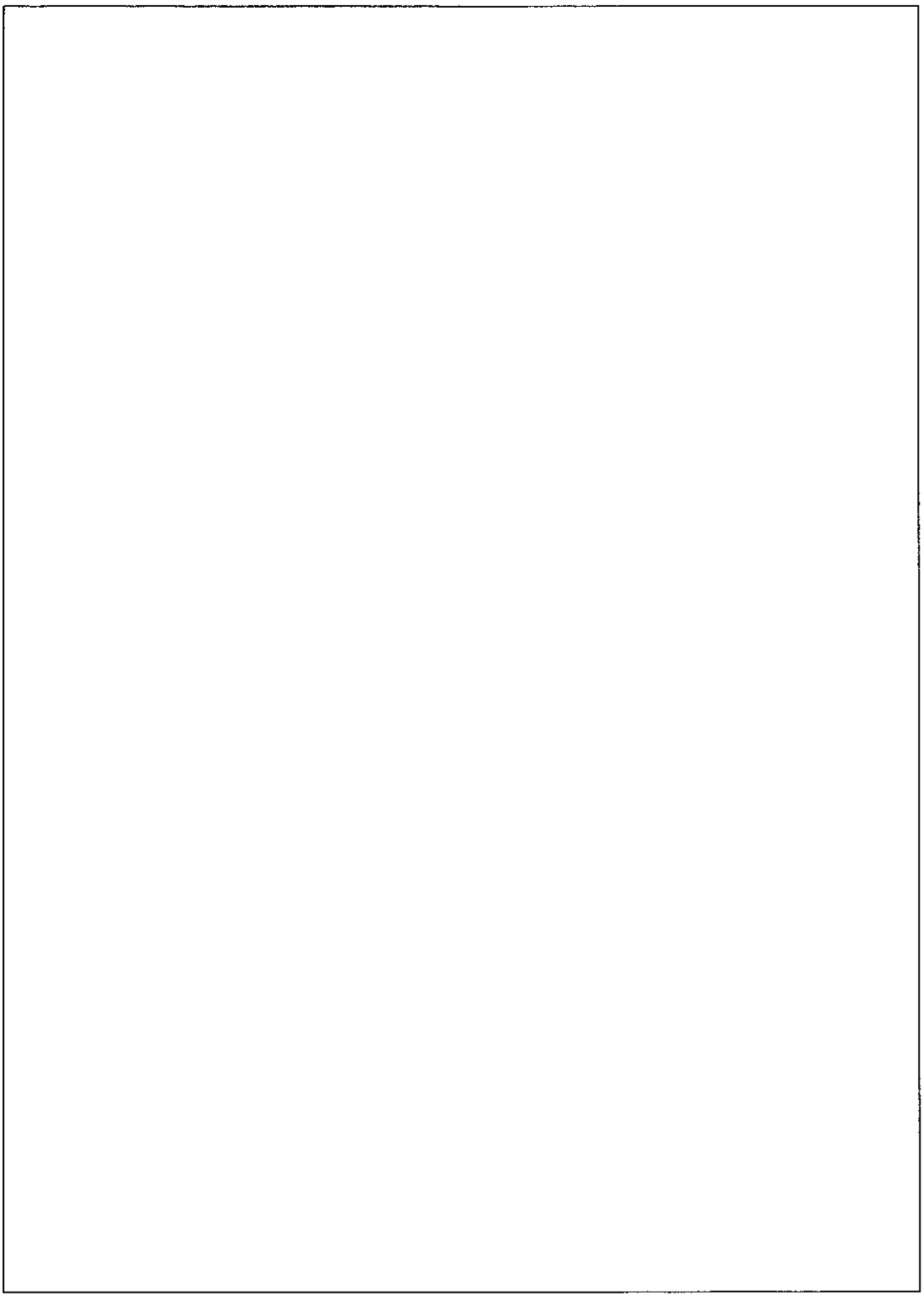
Electrical Characteristics (Continued)

Note 8: $T_A = 25°C$ and $V_{CC} = 5V$.

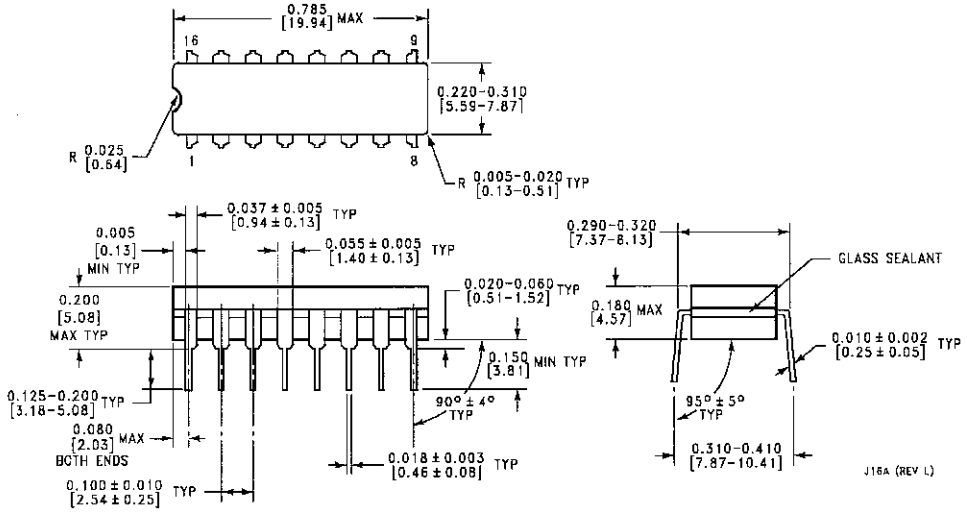
Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$

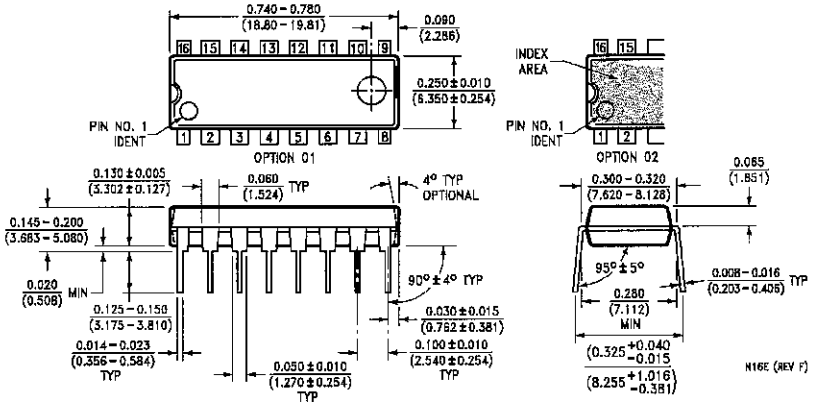
Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns



Physical Dimensions inches (millimeters) unless otherwise noted

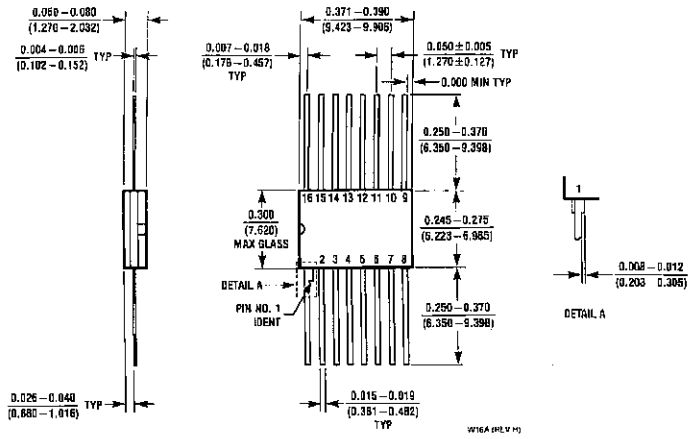


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 5476DMQB or DM5476J
Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM7476N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 5476FMQB or DM7476W
Package Number W16A

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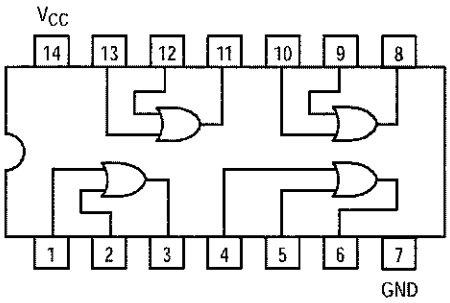
SN74LS32

Quad 2-Input OR Gate



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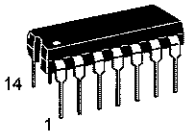
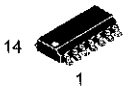
LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA



PLASTIC
N SUFFIX
CASE 646



SOIC
D SUFFIX
CASE 751A

ORDERING INFORMATION

Device	Package	Shipping
SN74LS32N	14 Pin DIP	2000 Units/Box
SN74LS32D	14 Pin	2500/Tape & Reel

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)	−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH			6.2	mA	V_{CC} = MAX	
	Total, Output LOW			9.8			

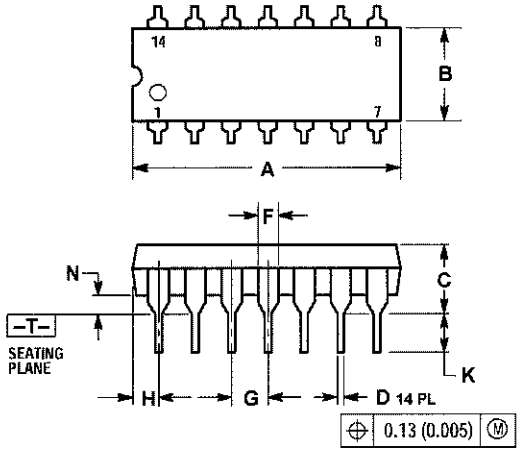
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn-Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		14	22	ns	

PACKAGE DIMENSIONS

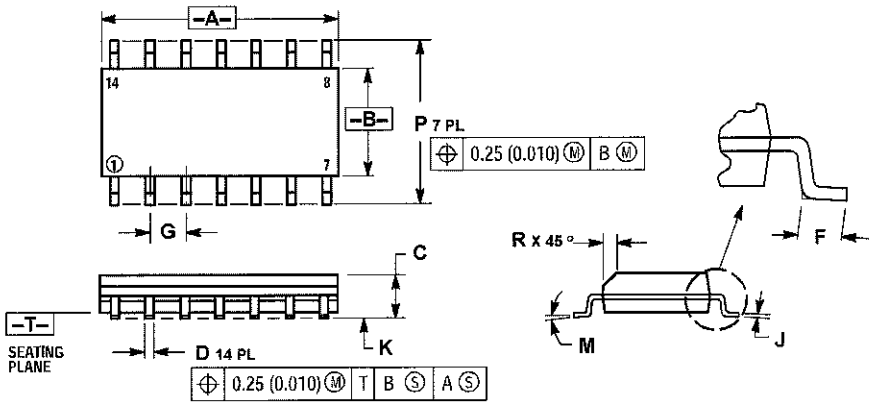
N SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	—	10°	—	10°
N	0.015	0.039	0.38	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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