FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE AND TECHNOLOGY

School of Electrical & Electronics Engineering

Bachelor of Engineering (Honours) Electrical/Electronics Engineering

EEB602 – Analog Electronics

FINAL EXAMINATION

Semester 1, 2019

Date: As per Exam Time Table

Time: As per Exam Time Table

Venue: As per Exam Timetable

Duration of Exam: 3 Hours

Total number of pages: 12

Instructions to Students

1. You are allowed an extra ten (10) minutes of reading time during which you are NOT allowed to write.
2. Attempt all questions.
3. Write your answers in the answer booklet provided.
4. Write your Student ID number on each page used.
5. Begin each Section on a fresh page and use both sides of the answer sheet.
6. You may use calculators provided they are non-programmable.
7. Clearly number the questions in your answer paper in their correct sequence and write legibly. Show all working.
8. Attach any extra sheets used to your answer booklet securely with the string provided.

****

Question 1 (20 marks)

a) Design an unregulated power supply with following specifications:
Input voltage: 240Vrms @60 Hz
Output voltage 16V dc ±10%
Ripple factor (max)= 3%
Load current(max) = 200mA.

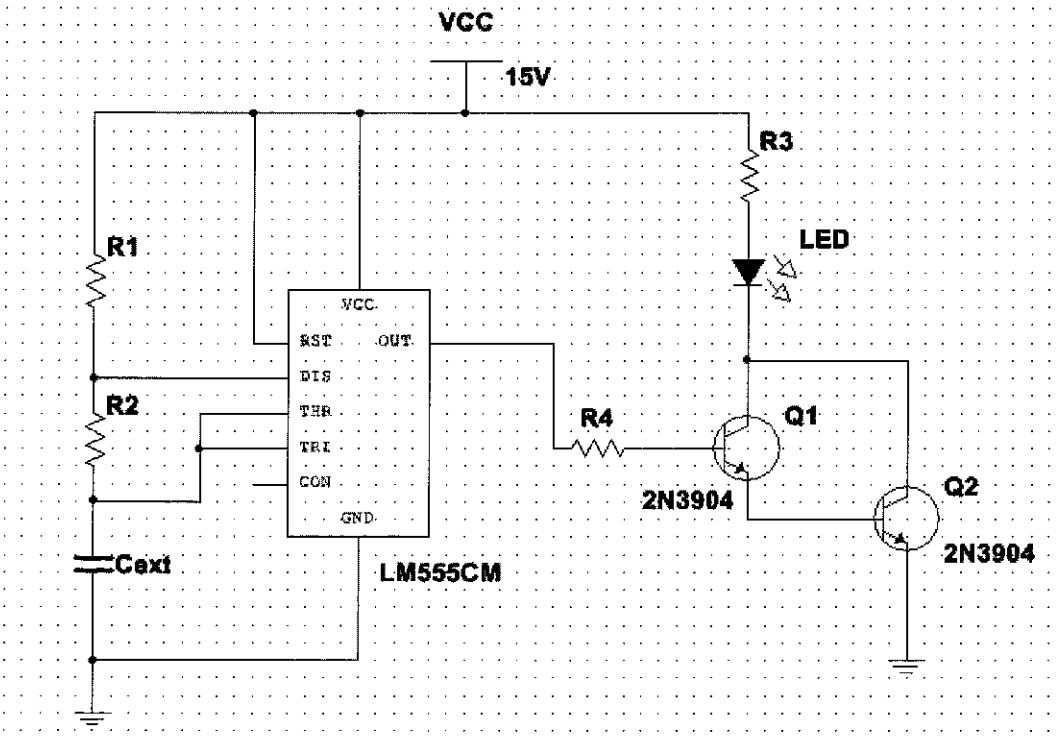
(8 marks)

b) Upgrade unregulated power supply of (a) to regulated power supply with fixed output of 10V. ***(4 marks)***

c) Design a dc bias circuit for an amplifier in which the voltage gain is to be a minimum of 50 and the output signal voltage is to be "riding" on a dc level of 5 V. The maximum input signal voltage at the base is 10 mV rms. $V_{CC} = 12\,V$, and $V_{BB} = 4$ V. Assume $r_e' = 8$ ohms. ***(8 marks)***

Question 2 (20 marks)

a) As an Electrical Engineer, you are given the task to design a circuit, which will turn on the LED for 1.2 milliseconds and then will turn off the LED for 0.8 milliseconds and the cycle continues. You are given the following circuit and the requirements are outlined:



Please Turn Over

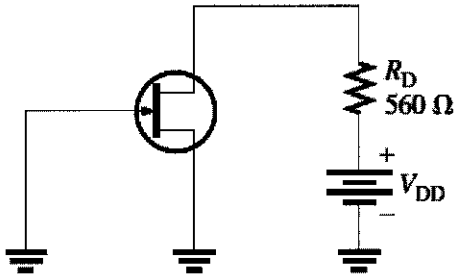
Requirements:

1. When the LED is on, its current should be 12mA. LED details are 10mm, V_f of 1.8V at minimum V_{cc}. Maximum forward current of 35mA.
2. LM555 produces 5V peak output. Other details and formulas of LM555 are available in appendix section. $R_3 = 500\Omega$.

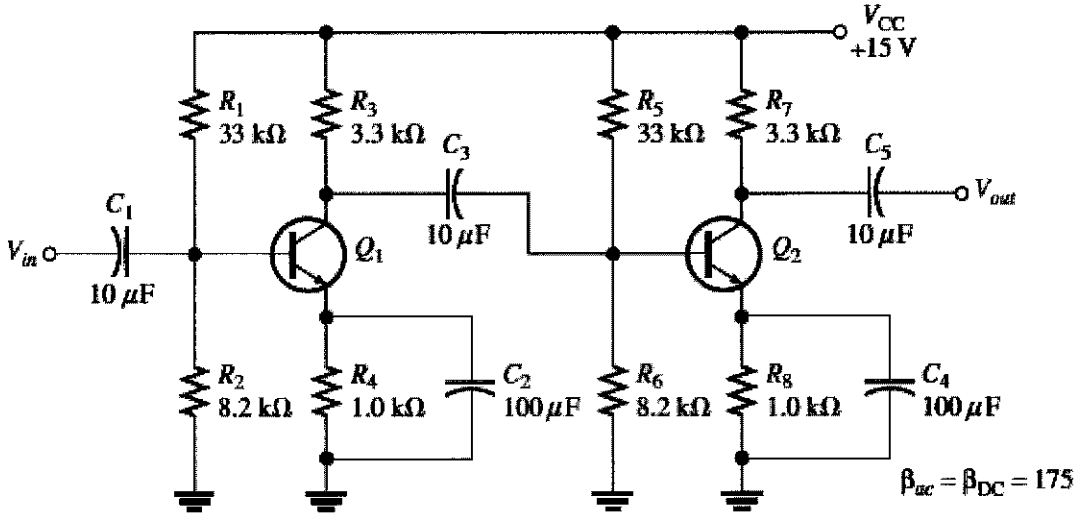
(8 marks)

b) Draw the biasing circuit of n-channel JFET and describe the basic operation. ***(4 marks)***

c) For the JFET in Figure below $V_{GS(off)} = -4V$ and $I_{DSS} = 12mA$. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation, when $V_{GS} = 0$. ***(4 marks)***



d) For the circuit given below, compute the overall gain. ***(4 marks)***



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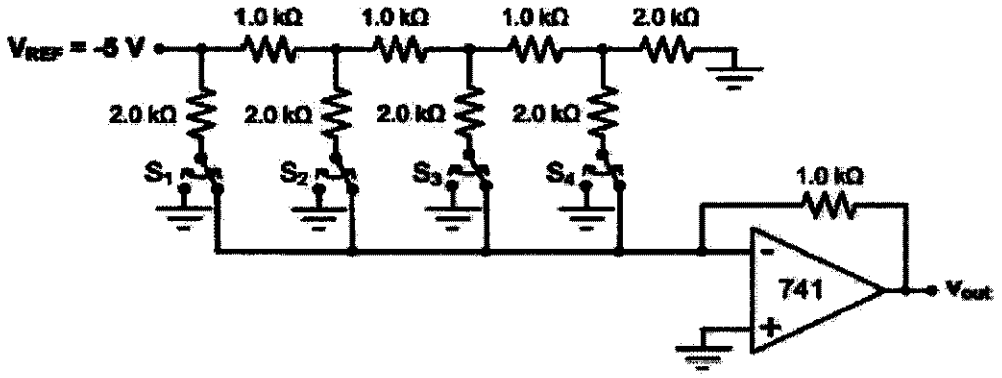
Question 3 (20 marks)

a) Compute the output voltage when the digital inputs are 0011 and 0100 in the circuit below. *(4 marks)*



b) To design a dual-slope ADC to digitize an anlog signal with a 10V range. We have 20MHz clock available, and the power supplies are $\pm$10V. The quantization error must be $\leq$ 5mV.

i) How many bits are required for the ADC. *(3 marks)*

ii) What is the maximum frequency input signal that can be digitized while meeting the Nyquist sampling rate requirements? *(3 marks)*

c) For the circuit shown on next page, answer the following questions:

i) Compute the gain of each stage. *(3 marks)*

ii) Determine the peak output voltage at points X, Y and Z. *(4 marks)*

iii) Draw the output voltage waveform at point Z, when switches S1 and S2 are closed. Consider practical diodes. *(3 marks)*

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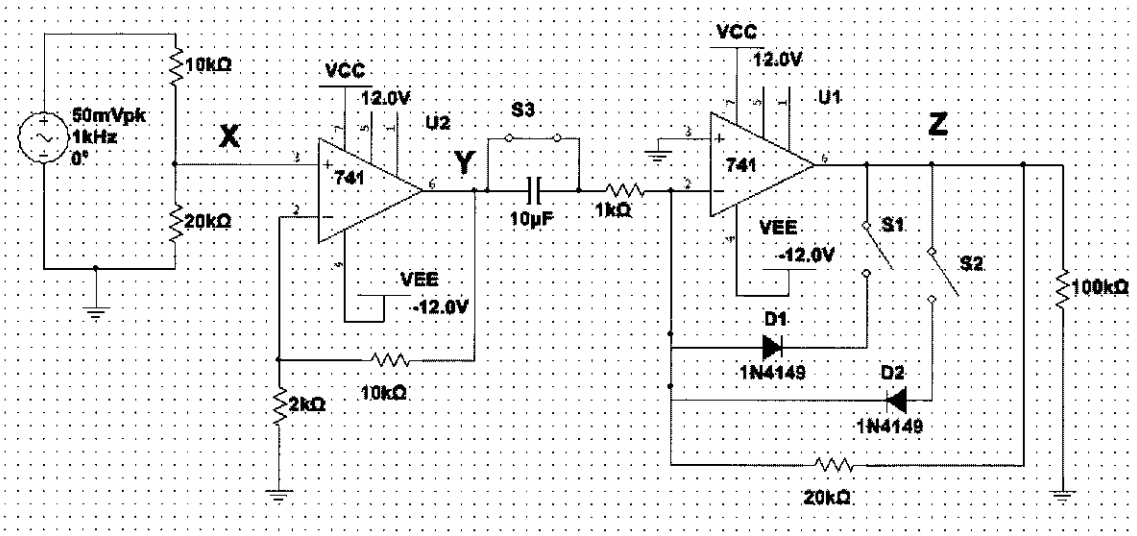

Question 4 (20 marks)

a) The gain of a certain amplifier as a function of frequency is $A(j\omega) = \frac{-16 \times 10^6}{j\omega}$. A feedback path connected around it has $\beta(j\omega) = \frac{10^3}{(2\times10^3+jw)^2}$. Will the system oscillate? If so, at what frequency. ***(6 marks)***

b) Compare the characteristics of classes A, B, AB and C power amplifiers ***(6 marks)***

c) Design a Wien bridge oscillator circuit with an oscillation frequency of 2.1 kHz. Add a relevant amplitude stabilization circuit to achieve sustained oscillation. The oscillation amplitude is to be 8.2 volts peak. ***(8 marks)***

Question 5 (20 marks)

a) As an Engineer, you are given the task to design a Butterworth Band-Pass filter with the following requirements:

- -3 dB bandwidth
- Roll-off rates of -40dB/decade
- Upper frequency of 15kHz and lower frequency of 10kHz

(10 marks)

b) Describe the purpose of multi-stage amplifiers and outline the characteristics of first stage, middle stage and last stage. ***(5 marks)***

c) Determine the gate trigger current and the anode current when the switch, SW1, is momentarily closed in Figure on the next page. Assume V_{AK} =0.2V, V_{GK} =0.7V and I_H=5mA. ***(5 marks)***

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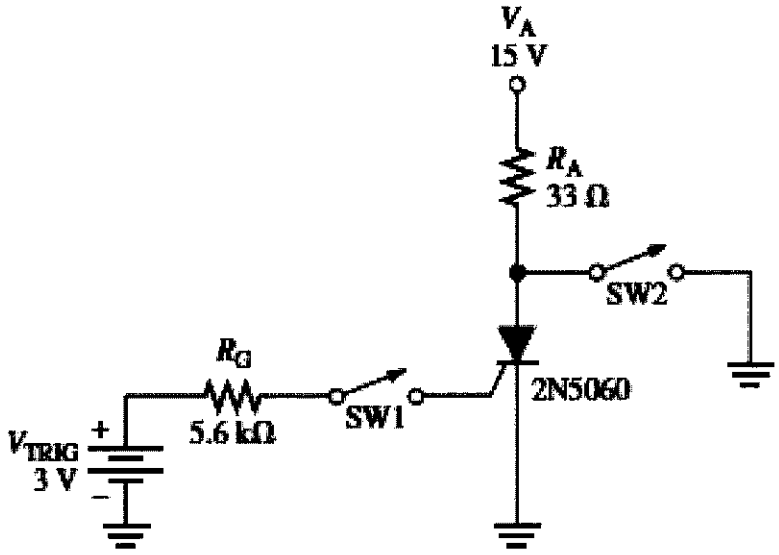

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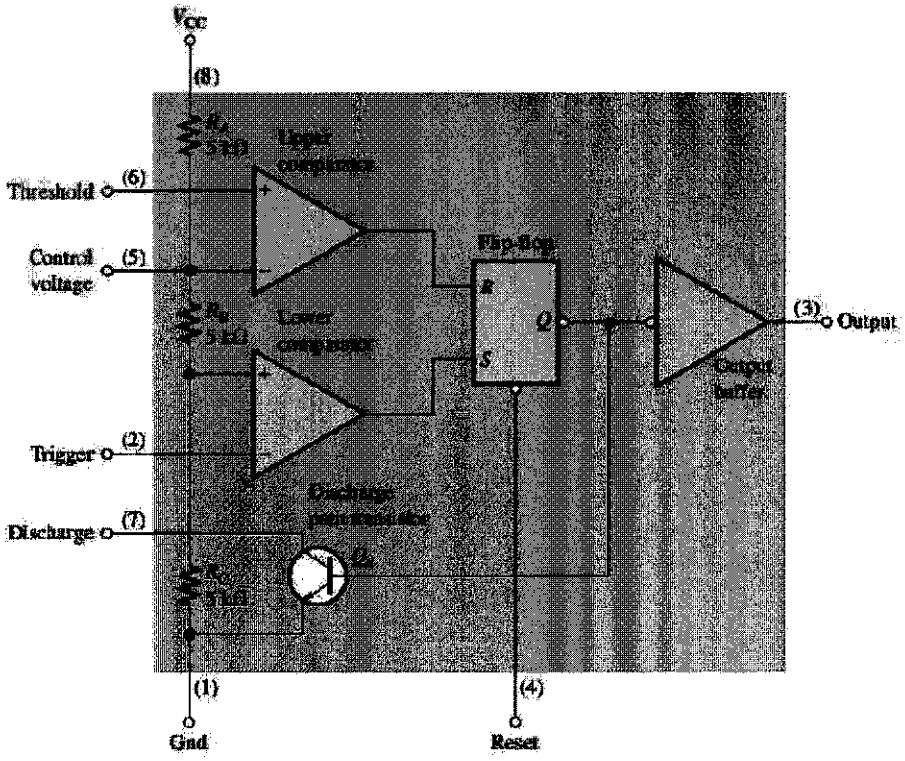
APPENDIX

Butterworth response.

ORDER	ROLL-OFF DB/DECADE	1ST STAGE POLES	DF	R_1/R_f	2ND STAGE POLES	DF	R_1/R_f	3RD STAGE POLES	DF	R_1/R_f

Internal diagram of a 555 integrated circuit timer and Formulas



$$f_r = \frac{1.44}{(R_1 + 2R_2)C_{ext}}$$

$$Duty\ Cycle = \left(\frac{t_H}{t_H + t_L}\right)100\% = \left(\frac{R_1 + R_2}{R_1 + 2R_2}\right)100\%$$

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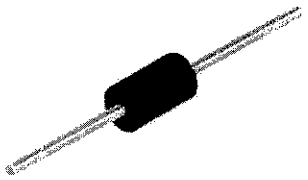


DO-41
COLOR BAND DENOTES CATHODE

Absolute Maximum Ratings * T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current .375 " lead length @ T_A = 75°C	1.0							A
I_{FSM}	Non-Repetitive Peak Forward Surge Current 8.3ms Single Half-Sine-Wave	30							A
I^2t	Rating for Fusing (t<8.3ms)	3.7							A^2sec
T_{STG}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

* These ratings are limiting values above which the serviceability of any semiconductor device may by impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

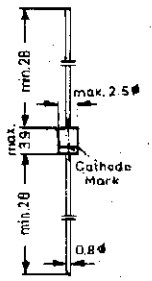
Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_F	Forward Voltage @ 1.0A	1.1	V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30	µA
I_R	Reverse Current @ Rated V_R T_A = 25°C T_A = 100°C	5.0 50	µA µA
C_T	Total Capacitance V_R = 4.0V, f = 1.0MHz	15	pF

1N4729 THRU 1N4764

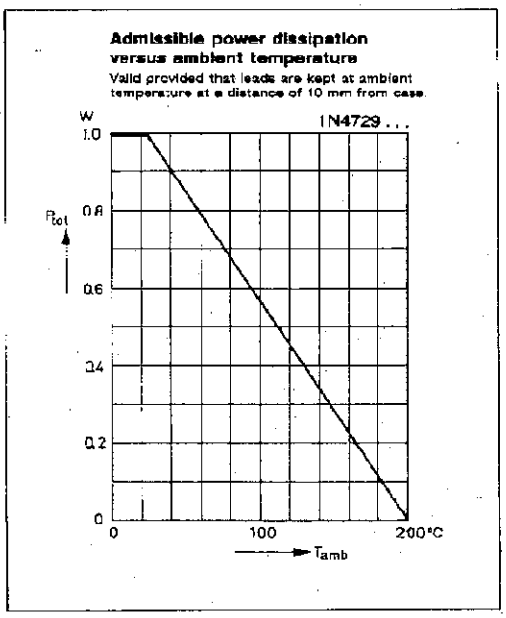
SILICON PLANAR POWER ZENER DIODES

Silicon Planar Power Zener Diodes
for use in stabilizing and clipping circuits with high power rating. Standard Zener voltage tolerance is ±10 %. Add suffix "A" for ±5 % tolerance. Other tolerances available upon request.



Glass case ≈ JEDEC DO-41

Dimensions in mm



Absolute Maximum Ratings

	Symbol	Value	Unit
Zener Current see Table "Characteristics"			
Power Dissipation at T_{amb} = 25 °C	P_{tot}	1[1]	W
Junction Temperature	T_j	200	°C
Storage Temperature Range	T_s	−65 to +200	°C
[1] Valid provided that leads at a distance of 10 mm from case are kept at ambient temperature			

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	170[1]	K/W
Forward Voltage at I_F = 200 mA	V_F	–	–	1.2	V
[1] Valid provided that leads at a distance of 10 mm from case are kept at ambient temperature					

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1N4729 THRU 1N4764

Type	Nominal Zener voltage[3] at I_{ZT} V_Z V	Test current I_{ZT} mA	Maximum Zener impedance[1] at I_{ZT} Z_{ZT} Ω	Z_{ZK} Ω	at I_{ZK} mA	Maximum reverse leakage current I_R µA	at V_R V	Surge current at T_A = 25°C I_R mA	Maximum regulator current[2] I_{ZM} mA
1N4729	3.6	69	10	400	1.0	100	1	1260	252
1N4730	3.9	64	9	400	1.0	100	1	1190	234
1N4731	4.3	58	9	400	1.0	50	1	1070	217
1N4732	4.7	53	8	500	1.0	10	1	970	193
1N4733	5.1	49	7	550	1.0	10	1	890	178
1N4734	5.6	45	5	600	1.0	10	2	810	162
1N4735	6.2	41	2	700	1.0	10	3	730	146
1N4736	6.8	37	3.5	700	1.0	10	4	660	133
1N4737	7.5	34	4.0	700	0.5	10	5	605	121
1N4738	8.2	31	4.5	700	0.5	10	6	550	110
1N4739	9.1	28	5.0	700	0.5	10	7	500	100
1N4740	10	25	7	700	0.25	10	7.6	454	91
1N4741	11	23	8	700	0.25	5	8.4	414	83
1N4742	12	21	9	700	0.25	5	9.1	380	76
1N4743	13	19	10	700	0.25	5	9.9	344	69
1N4744	15	17	14	700	0.25	5	11.4	304	61
1N4745	16	15.5	16	700	0.25	5	12.2	285	57
1N4746	18	14	20	750	0.25	5	13.7	250	50
1N4747	20	12.5	22	750	0.25	5	15.2	225	45
1N4748	22	11.5	23	750	0.25	5	16.7	205	41
1N4749	24	10.5	25	750	0.25	5	18.2	190	38
1N4750	27	9.5	35	750	0.25	5	20.6	170	34
1N4751	30	8.5	40	1000	0.25	5	22.8	150	30
1N4752	33	7.5	45	1000	0.25	5	25.1	135	27
1N4753	36	7.0	50	1000	0.25	5	27.4	125	25
1N4754	39	6.5	60	1000	0.25	5	29.7	115	23
1N4755	43	6.0	70	1500	0.25	5	32.7	110	22
1N4756	47	5.5	80	1500	0.25	5	35.8	95	19
1N4757	51	5.0	95	1500	0.25	5	38.8	90	18
1N4758	56	4.5	110	2000	0.25	5	42.6	80	16
1N4759	62	4.0	125	2000	0.25	5	47.1	70	14
1N4760	68	3.7	150	2000	0.25	5	51.7	65	13
1N4761	75	3.3	175	2000	0.25	5	56.0	60	12
1N4762	82	3.0	200	3000	0.25	5	62.2	55	11
1N4763	91	2.8	250	3000	0.25	5	69.2	50	10
1N4764	100	2.5	350	3000	0.25	5	76.0	45	9

[1] The Zener Impedance is derived from the 60 Hz AC voltage which results when an AC current having an RMS value equal to 10 % of the Zener current (I_{ZT} or I_{ZK}) is superimposed on I_{ZT} or I_{ZK}. Zener Impedance is measured at two points to insure a sharp knee on the breakdown curve and to eliminate unstable units.

[2] Valid provided that leads at a distance of 10 mm from case are kept at ambient temperature.

[3] Measured under thermal equilibrium and DC test conditions.

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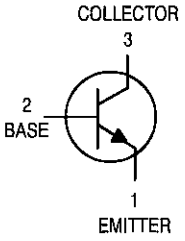
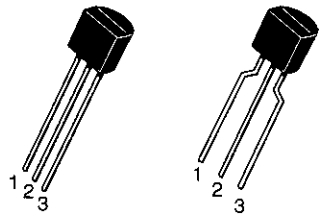


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CBO}	60	Vdc
Emitter−Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 1.5 12	 W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

TO−92
CASE 29
STYLE 1



STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

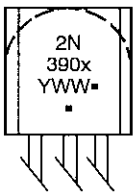
THERMAL CHARACTERISTICS (Note 1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates Data in addition to JEDEC Requirements.

MARKING DIAGRAMS



x = 3 or 4
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (Note 2) (I_C = 1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	40	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		$V_{(BR)CBO}$	60	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	6.0	–	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{BL}	–	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{CEX}	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (Note 2)		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3903		20	–	
	2N3904		40	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903		35	–	
	2N3904		70	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903		30	–	
	2N3904		60	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903		15	–	
	2N3904		30	–	
Collector–Emitter Saturation Voltage (Note 2)		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			–	0.2	
(I_C = 50 mAdc, I_B = 5.0 mAdc			–	0.3	
Base–Emitter Saturation Voltage (Note 2)		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	0.95	
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain – Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3903		250	–	
	2N3904		300	–	
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	–	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	–	8.0	pF
Input Impedance		h_{ie}			k Ω
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		1.0	8.0	
	2N3904		1.0	10	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		0.1	5.0	
	2N3904		0.5	8.0	
Small–Signal Current Gain		h_{fe}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		50	200	
	2N3904		100	400	
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	1.0	40	μmhos
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N3903		–	6.0	
	2N3904		–	5.0	

SWITCHING CHARACTERISTICS

Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc, I_C = 10 mAdc, I_{B1} = 1.0 mAdc)	t_d	–	35	ns
Rise Time		t_r	–	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1.0 mAdc) 2N3903	t_s	–	175	ns
	2N3904		–	200	
Fall Time		t_f	–	50	ns

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.