FNU FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE & TECHNOLOGY (CEST)

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

CERTIFICATE III IN ELECTRONIC ENGINEERING

CERTIFICATE IV IN ELECTRONIC ENGINEERING

EEC309- DIGITAL ELECTRONICS I

FINAL EXAMINATION – QUARTER 2, 2019

DATE: As per timetable **TIME:** As per timetable

TIME ALLOWED: 2 HOURS 10 MINUTES

INSTRUCTIONS TO STUDENTS

1. *You are allowed 10 minutes extra reading time during which you are NOT to write.*
2. *Begin each section on a new page and use both sides of the sheet.*
3. *Write your candidate-number at the top of each attached sheet.*
4. *Insert all written foolscaps, graph paper, drawing paper, etc. in their correct sequence and secure with string.*
5. *For all sheets of paper on which rough/draft work has been done, cross each one through and ATTACH these to your answer scripts.*
6. *Write clearly the number(s) of the question(s) attempted on the top of each sheet.*
7. *Show all working clearly where necessary.*
8. *Programmable calculators are not allowed, especially the ones that do the conversions of number systems.*
9. *Always check your work before leaving the exam hall.*
10. *Answer all questions.*

Section A – Multiple Choice [10 marks]

Choose the appropriate answer from each question by writing the alphabet beside the question number in your answer booklet.

1. One of the advantages of digital over analog representation is that;
   A. Data can be processed and transmitted more efficiently and reliably.
   B. Digital signals typically use less bandwidth.
   C. Data cannot become corrupted.
   D. Output is not subject to quantity errors from sampling

2. The SOP form of the Boolean expression AB + B(CD + EF) is;
   A. (A + B)(BCD + BEF)
   B. AB + BCD + BEF
   C. (A + B)(B + C + D)(B + E + F)
   D. AB(B+C+D)(B+E+F)

3. The binary number for $F7A9_{16}$ is
   A. 1111011110101001
   B. 1110111110101001
   C. 1111111010110001
   D. 1111011010101001

4. What is the weight of digit 6 in the decimal number 1386?
   A. 1
   B. 2
   C. 3
   D. 0

5. The Boolean expression for a 3-input AND gate is;
   A. A + B + C
   B. ABC
   C. AB + C
   D. A x B + C

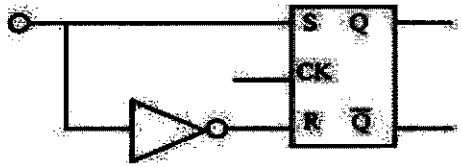
6. What is the total number of possible combinations of binary inputs to a gate having three input variables?
   A. 2
   B. 4
   C. 8
   D. 16

Please Turn Over

7. The output of an exclusive-OR gate is HIGH when;
   A. all inputs are LOW
   B. all inputs are HIGH
   C. the inputs are unequal
   D. none of the above

8. How is a *J-K* flip-flop made to toggle?
   A. J = 0, K = 0
   B. J = 1, K = 1
   C. J = 1, K = 0
   D. J = 0, K = 1

9. Identify the type of Flip Flop the Logic Gate circuit represents;
   A. MS Flip Flop
   B. SR Flip Flop
   C. T Flip Flop
   D. D Flip Flop



10. The Boolean expression $A+\overline{B}+C$ is a;
    A. Sum term
    B. Literal term
    C. Product term
    D. Complemented term

Section B – Number Systems & Logic Gates [30 marks]

Show ALL working clearly where required. Answer all questions.

1. Draw the switch equivalent circuit for an OR Gate. (2 marks)

2. Explain the following threshold voltage acronyms;
   A. V_{IH} (1 mark)
   B. V_{OL} (1 mark)

3. Convert the decimal number 45.5 to binary by using the sum-of-weights method. (2 marks)

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4. Convert the decimal number 57 to the following numbers using any of the conversion methods.
   A. Binary number (2 marks)
   B. Hexadecimal number (2 marks)
   C. Octal number (2 marks)

5. Convert the following to octal;
   A. $3A516_{16}$ (2 marks)
   B. 110101111_2 (2 marks)

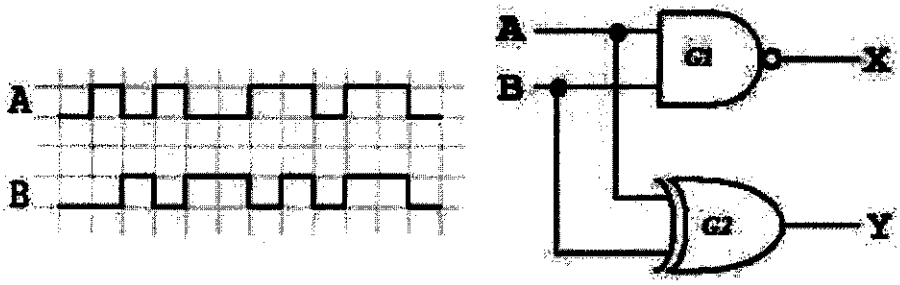
6. What is the largest decimal number that can be represented in binary with eight bits? (1 mark)

7. Describe the operation of a 3 input OR gate. (2 marks)

8. Convert the binary number 11000110 to Gray code. (2 marks)

9. What is a Truth Table? Explain clearly. (2 marks)

10. Using the figure below, answer the following questions.



   A. Name the gates labeled G1 and G2. (1 mark)
   B. Draw the truth tables of gates G1 and G2. (2 marks)
   C. Determine the output waveforms X and Y, given the input signals A and B as above. (4 marks)

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Section C – Boolean Algebra & Logic Simplifications [30 marks]

Show ALL working clearly where required. Answer all questions.

1. State DeMorgan's theorem. (2 marks)

2. Convert the Boolean expression, $\overline{\overline{(A+B)}+C}$ to SOP form. (2 marks)

3. Apply DeMorgan's theorem to each expression;
   A. $\overline{(A+B+C)D}$ (2 marks)
   B. $\overline{\overline{(A+B)}+\overline{C}}$ (2 marks)

4. Using Boolean algebra techniques, simplify this expression;
   A. $AB+A(B+C)+B(B+C)$ (3 marks)
   B. $(A+\overline{B})(A+C)$ (3 marks)
   C. $AB+(\overline{A}+\overline{B})C+AB+\overline{B}C$ (2 marks)

5. Draw a truth table for the standard SOP expression; $A\overline{B}C+\overline{A}\overline{B}\overline{C}+ABC$. (2 marks)

6. Identify the law of Boolean algebra upon which each of the following equalities is based;
   A. $A\overline{B}+CD+A\overline{C}D+B=B+A\overline{B}+A\overline{C}D+CD$ (1 mark)
   B. $AB(CD+E\overline{F}+GH)=ABCD+ABE\overline{F}+ABGH$ (1 mark)

7. Convert the Boolean expression, $A\overline{B}C+\overline{A}\overline{B}+AB\overline{C}D$, into standard SOP form. (2 marks)

8. What is the minimum POS expression derived from the Karnaugh map shown below? (3 marks)

WX \ YZ	00	01	11	10
00				
01	0	0		
11			0	0
10	0	0	0	0

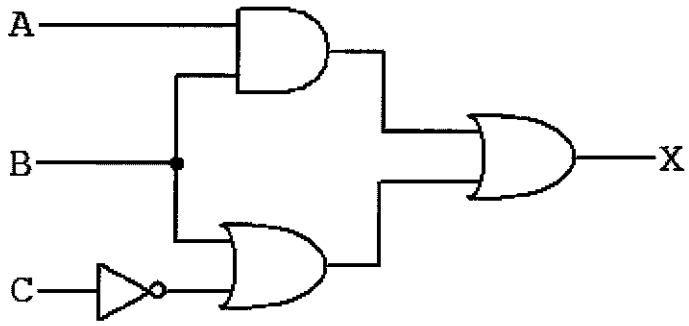
Please Turn Over

9. Develop a truth table for the POS expression; $(\overline{A}+\overline{B}+\overline{C})(A+B+C)(A+\overline{B}+C)$ (2 marks)
10. Use the Karnaugh map to find the minimum SOP form for the expression; $\overline{A}\overline{B}\overline{C}+A\overline{B}\overline{C}+\overline{A}B\overline{C}+AB\overline{C}$. (3 marks)

Section D – Combinational & Sequential Circuits [30 marks]

Show ALL working clearly where required. Answer all questions.

1. What do you understand by the term "Positive Edge Triggered Flip-flop"? (2 marks)
2. Operating characteristics of flip-flops specify the performance, operating requirements, and operating limitations of the circuit. What do you understand by the following terms that is usually specified in the datasheets of the flip-flops;
   A. Propagation Delay Time (2 marks)
   B. Power Dissipation (2 marks)
3. Determine the expression at X for the following circuit.



(2 marks)

4. Flip-flops can be connected together to perform counting operations. Such a group of flip-flops is a counter.
   A. Draw the circuit of a mod-12 ripple counter using JK Flip-flops for the clock triggering on the rising edge. Show all circuit connections and label the pins clearly. (5 marks)
   B. Draw the timing diagram for the Q outputs of all flip-flops for twelve clock pulses. (8 marks)

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5. Sensors A, B, and C controls the conveyor belt Q, in a sugar mill. The conveyor must operate if sensor A is ON and B is ON but C is OFF; or if A is OFF, B is ON and C is ON; or if A is ON, B is OFF and C is ON. Under all other conditions the conveyor must NOT operate.
   A. Determine the truth table for all possible combinations of the three sensors. (3 marks)
   B. Write the Boolean expression for which the conveyor belt is operational. (2 marks)
   C. Draw the logic circuit to show this operation. Use a LED to indicate the status of the conveyor belt. (4 marks)

The End

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