FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE AND TECHNOLOGY
SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

DIPLOMA IN ENGINEERING: ELECTRONICS
(INSTRUMENTATIONS & CONTROL)
(TELECOMMUNICATIONS & NETWORKING)

EED506 DIGITAL ELECTRONICS

SUPPLEMENTARY ASSESSMENT – FINAL EXAMINATION (QUARTER 3, 2019)

DATE/TIME/ROOM – Refer to Exam Timetable
(3 hours + 10 minutes)

INSTRUCTIONS TO CANDIDATES

1. You are allowed 10 minutes extra time during which you are not to write.
2. Write all your answers in the allocated Answer Booklet.
3. Begin each answer on a fresh new page and use both sides of the sheets.
4. Write your identification number on the top of each attached sheet.
5. Insert all written foolscaps, graph paper, drawing paper, etc in their correct sequence and secure with string provided.
6. For all sheets of paper in which has been done, cross it through and you must attach to your answer script.
7. Write clearly the number(s) of the question(s) attempted on the top of each sheet.
8. Programmable and numbering system calculators are PROHIBITED.
9. All questions are compulsory and equates to 100 marks.

Section A: Multiple Choice (20 marks)

1. The resolution of an n bit DAC with a maximum input of 5 V is 5 mV. The value of n is .....
   a) 8
   b) 9
   c) 10
   d) 11

(1 mark)

2. A decade counter skips .....
   a) Binary states 1000 to 1111
   b) Binary states 0000 to 0011
   c) Binary states 1111 to higher
   d) Binary states 1010 to 1111

(1 mark)

3. BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are .....
   a) a, b, d
   b) All
   c) a, b, g, c, d
   d) None

(1 mark)

4. A ring counter with 5 flipflops will have ..... states.
   a) 5
   b) 10
   c) 32
   d) Infinite

(1 mark)

5. ..... has one input and many outputs.
   a) Multiplexer
   b) Demultiplexer
   c) Counter
   d) Flipflop

(1 mark)

6. For the minterm designation $Y = \sum m(1, 3,5,7)$ the complete expression is .....
   a) $Y = \bar{A}\bar{B}C + A\bar{B}C$
   b) $Y = \bar{A}\bar{B}C + A\bar{B}C + ABC + \bar{A}BC$
   c) $Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C$
   d) $Y = \bar{A}\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C + A\bar{B}C$

(1 mark)

7. Maximum number of inputs (load) that can be connected to output of a gate without degrading normal operation is:
    a) Fan-out
    b) Fan-in
    c) Fan-high
    d) Fan-low

(1 mark)

8. How many outputs are on a BCD decoder?
    a) 4
    b) 16
    c) 8
    d) 10

(1 mark)

9. In the sum of products function $f(X,Y,Z) = \sum(2,3,4,5)$, the prime implicants are:
    a) $\bar{X}Y, X\bar{Y}$
    b) $\bar{X}Y, X\bar{Y}\bar{Z}, X\bar{Y}Z$
    c) $\bar{X}Y\bar{Z}, \bar{X}YZ, X\bar{Y}$
    d) $\bar{X}Y\bar{Z}, \bar{X}YZ, X\bar{Y}\bar{Z}, X\bar{Y}Z$

(1 mark)

10. A 8-input AND gate has a fan-out of:
    a) 1
    b) 4
    c) 8
    d) 12

(1 mark)

11. For higher speed and better density, resistors used in RTL were replaced by:
    a) MOSFETs
    b) Resistors
    c) Capacitors
    d) Diodes

(1 mark)

12. For standard TTL (known as 74 series), low input level 'V_{IL}' is:
    a) 0.8 V
    b) 1 V
    c) 1.8 V
    d) 2 V

(1 mark)

13. Simplest line decoder is:
    a) 0 – 1 line decoder
    b) 1 – 2 line decoder
    c) 0 – 2 line decoder
    d) 1 – 5 line decoder

(1 mark)

14. A 16-input multiplexer is to be used to perform parallel-to-serial data conversion. Which of the following counters would be required to provide the data select inputs?
    a) MOD 8
    b) MOD 16
    c) MOD 4
    d) MOD 2

(1 mark)

15. In DTL logic gating function is performed by _____
    a) Diode
    b) Transistor
    c) Inductor
    d) Capacitor

(1 mark)

16. A 16:1 multiplexor uses _____ selector bits.
    a) 1
    b) 2
    c) 3
    d) None of the above

(1 mark)

17. Propagation delay is defined as _____
    a) the time taken for the output of a gate to change after the inputs have changed
    b) the time taken for the input of a gate to change after the outputs have changed
    c) the time taken for the input of a gate to change after the intermediates have changed
    d) the time taken for the output of a gate to change after the intermediates have changed

(1 mark)

18. A device that sets a logical 1 on one output line while other lines are kept at logical 0 is a:
    a) Latch
    b) Active-High decoder
    c) Multiplexor
    d) Active-Low decoder

(1 mark)

19. Transistor-transistor logic (TTL) is a class of digital circuits built from _____
    a) JFET only
    b) Bipolar Junction transistors (BJT)
    c) Resistors
    d) BJT and resistors

(1 mark)

20. If two inputs are active on a priority encoder, which will be coded on the output?
    a) The higher value
    b) The lower value
    c) Neither of the inputs
    d) Both of the inputs

(1 mark)

Section B (80 marks)

Question 1: Combinational Logic Circuit – Minimisations (20 marks)

Design a multiple-output logic network whose input is a BCD digit and when outputs are defined as follows:

- F1: detects input digits of multiples of 2 that are divisible by 2
- F2: detects numbers greater than or equal to 5
- F3: detects numbers less than 4

a) State the condition and status of this design. (3 marks)

b) Implement the truthtable to illustrate the operation of this design. (7 marks)

c) Minimise part c) using karnaugh mapping. (6 marks)

d) Sketch the minimised Boolean Equation logic diagram. (4 marks)

Question 2: MSI Combinational Logic Devices and systems (10 marks)

Use 74151 MUX to build the following system folded about X_1

X_4	X_3	X_2	X_1	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

a) Develop its truthtable (6 marks)

c) Sketch the IC showing the realization (4 marks)

Question 3: Synchronous Counters (30 marks)

Design mod-6 synchronous counter using JK Flip Flops. Check for the lock out condition. If so, how the lock-out condition can be avoided? Draw a neat state diagram and circuit diagram with Flip Flops. (2 + 6 + 4 + 4 + 4 + 5 + 5 = 30 marks)

Question 4: Display devices (10 marks)

a) Each segment of a typical 7-segment LED display is rated to operate at 5 mA at 2.1V for normal brightness. Calculate the value of the current-limiting resistor needed to produce approximately 5 mA per segment. (2 marks)

b) Refer to Appendix 1 showing the 7447 datasheet:

i. How does one test all LEDs of a seven segment display are in working order? (1 mark)

ii. Using the calculated R_s of part a); sketch the circuit diagram showing the 7447 decoder connected to a common anode 7-segment display. (7 marks)

Question 5: Programmable Logic Devices Architecture (10 marks)

a) List any two types of programmable logic devices. (2 marks)

b) Using Programmable Logic Array, implement the following functions:

- $F_1 = ABC$
- $F_2 = A + B + C$
- $F_3 = \bar{A}\bar{B}\bar{C}$
- $F_4 = \bar{A} + \bar{B} + \bar{C}$
- $F_5 = A\ xor\ B\ xor\ C$
- $F_6 = \overline{(A\ xnor\ B\ xnor\ C)}$ (8 marks)

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Appendix 1: 7447 MSI IS Datasheet

SN74LS47

BCD to 7-Segment Decoder/Driver

The SN74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250 µA. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Open Collector Outputs
- Lamp Test Provision
- Leading/Trailing Zero Suppression
- Input Clamp Diodes Limit High-Speed Termination Effects

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

LOW POWER SCHOTTKY

PLASTIC
N SUFFIX
CASE 648

SOIC
D SUFFIX
CASE 751B

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High BI/RBO			–50	µA
I_{OL}	Output Current – Low BI/RBO BI/RBO			3.2	mA
$V_{O(off)}$	Off–State Output Voltage a to g			15	V
$I_{O(on)}$	On–State Output Current a to g			24	mA

ORDERING INFORMATION

Device	Package	Shipping
SN74LS47N	16 Pin DIP	2000 Units/Box
SN74LS47D	16 Pin	2500/Tape & Reel

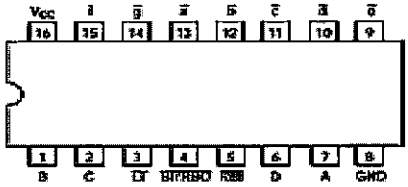
December, 1999 – Rev. 6

1

Publication Order Number:
SN74LS47/D

Pinouts :

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES		LOADING (Note a) HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple-Blanking Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp-Test Input	0.5 U.L.	0.25 U.L.
$\overline{BI/RBO}$	Blanking Input or	0.5 U.L.	0.75 U.L.
	Ripple-Blanking Output	1.2 U.L.	2.0 U.L.
$\overline{a}$ to $\overline{g}$	Outputs	Open-Collector	15 U.L.