FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE AND TECHNOLOGY

School of Electrical & Electronics Engineering

Bachelor of Engineering (Honours) (Electrical & Electronics Engineering)

EEB603 – Digital Electronics

SUPPLEMENTARY EXAMINATION

Semester 2, 2018

Date: As per Exam Time Table

Time: As per Exam Time Table (3 hours)

Venue: As per Exam Timetable

Instructions to Students

1. You are allowed an extra ten (10) minutes of reading time during which you are NOT allowed to write.
2. Attempt ALL questions in this examination booklet
3. Write your answers in the answer booklet provided.
4. Write your Student ID number on each page used.
5. Begin each Section on a fresh page and use both sides of the answer sheet.
6. You may use calculators provided they are non-programmable.
7. Clearly number the questions in your answer paper in their correct sequence and write legibly. Show all working.
8. Attach any extra sheets used to your answer booklet securely with the string provided.

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Section A: Multiple Choices [7 marks]
Choose the letter of the BEST choice.

1. Output will be a LOW for any case when one or more inputs are LOW for a:

   a) OR gate
   b) NOT gate
   c) NOR gate
   d) AND gate

2. How is a J-K flip-flop made to toggle?

   a) J = 0, K = 0
   b) J = 1, K = 0
   c) J = 0, K =1
   d) J = 1, K = 1

3. Give the decimal value of binary number 10010.

   a) 6_{10}
   b) 9_{10}
   c) 18_{10}
   d) 20_{10}

4. FPGA is the acronym for _____.

   a) Flexible Programming [of] Generic Assemblies
   b) Field Programmable Generic Array
   c) Field Programmable Gate Array
   d) Field Programmer's Gate Assembly

5. The device used to convert a binary number to a 7-segment display format is the
   a) multiplexer
   b) encoder
   c) decoder
   d) register

6. Which of the following statements does NOT describe an advantage of digital technology?

   a) The values may vary over a continuous range.
   b) The circuits are less affected by noise.
   c) The operation can be programmed.
   d) Information storage is easy.

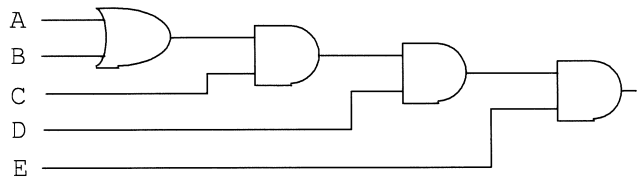
7. The hexadecimal equivalent of the binary number 111111110010 is:

   a) $EE2_{16}$
   b) $FF2_{16}$
   c) $2FE_{16}$
   d) $FD2_{16}$

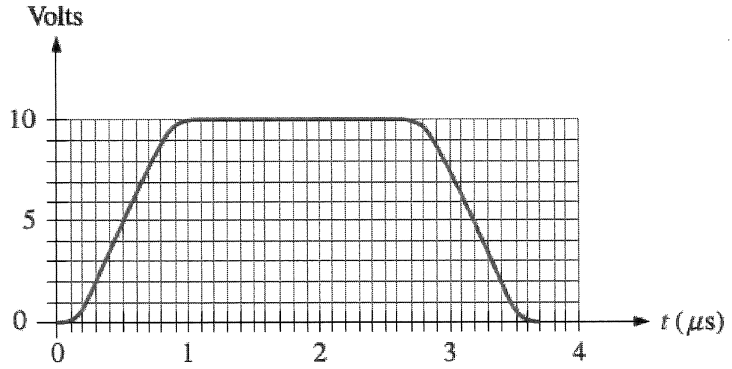
Please Turn Over

Section B: Short Answers (2 marks each) [14 marks]

1) Show the truth table of a 2 input XOR gate.
2) State the DeMorgan's theorems.
3) Convert the binary number 1001.00101 to decimal.
4) Derive the Boolean expression for the logic circuit shown below:



5) Convert the decimal number 57 to 8421 BCD.
6) If binary data are transferred on a USB at the rate of 480 million bits per second (480 Mbps), how long will it take to serially transfer 16 bits?
7) Determine the rise time for the pulse shown below.



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Section C: Concepts and Designing [79 marks]

Question 1: Number Systems [11 marks]

a) Represent the decimal number 42.625 in:

i) Binary [4 marks]

ii) Octal [3 marks]

b) Express the decimal number -25 in 8-bit sign magnitude number and 2's complement form. [4 marks]

Question 2: Logic Gates and Boolean Algebra [33 marks]

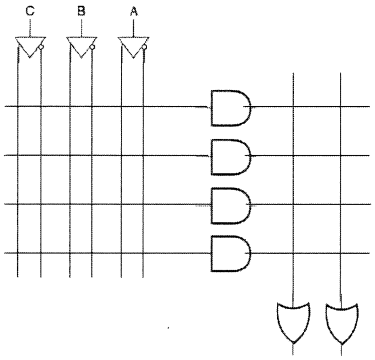
a) Using Boolean algebra techniques and DeMorgan's theorems, simplify the expression $\overline{\overline{A}+\overline{B}}+A(\overline{\overline{B}\,\overline{C}})+B(B+C)$ [3 marks]

b) A function F is given to be $F = A\overline{B} + AB\overline{C} + A\overline{B}C$.

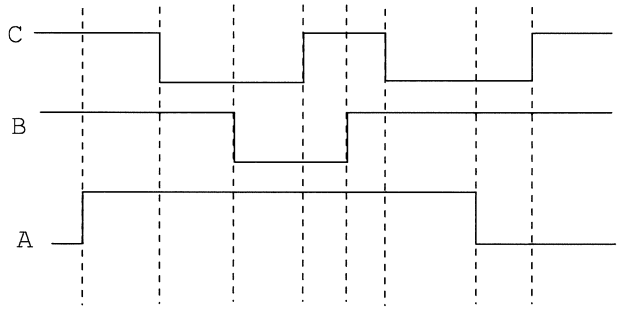
i) Show the truth table for this function (show all working). [3 marks]

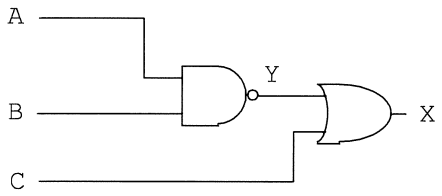
ii) Realize the circuit using minimum SOP expression (use Karnaugh map minimization). [3 marks]

iii) Implement the function F directly using the PLA given below. [2 marks]



c) Draw the output waveform for the four input system shown on the next page with its proper time relationship to the inputs. [4 marks]





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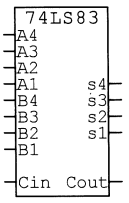
d) Given $f(A,B,C,D,E,F) = \sum_m (20,28,52,60)$, determine the minimum SOP expression using Quine-McClusky method. [8 marks]

e) Realize the function $X = (\overline{A} + \overline{B})CDE$ as stated using NAND gates only. [5 marks]

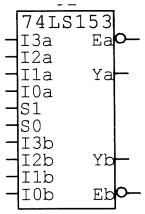
f) Realize the function $Y = \overline{\overline{A}\overline{B}\overline{C} + D + E}$ as stated using NOR gates only. [5 marks]

Question 3: Functions of Combinational Logic, MUX and DEMUX [10 marks]

a) Show how two 74LS83 adders can be connected to add the binary numbers 01110011 and 10010101. Show all input and output values. [4 marks]

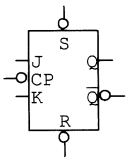


b) Realize the function $f(C,B,A) = \sum_m (0, 2, 4, 7)$ using the 74LS153 multiplexer. [6 marks]



Question 4: Flip-flops and Counters [25 marks]

a) Show how a modulus eleven asynchronous binary counter can be implemented using J-K flip-flops. [5 marks]



b) Given the following components (shown on the next page), design a synchronous counter using the given JK flip flops and logic gates that counts in the sequence: 7, 2, 5, 1, 3. The counter is to be self-starting and restart counting at 7 after 3. The final prototype must be a completely functional circuit which utilizes the 74LS47 BCD to 7 Segment Decoder/Driver. Select the correct 7 segment display to be used from the two given. [14 marks]

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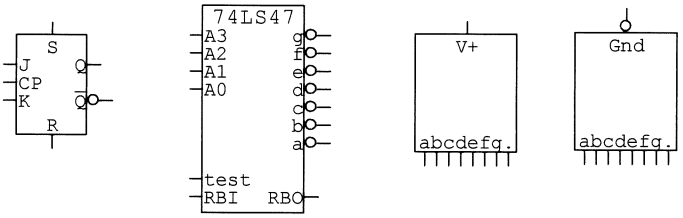

c) Write the hardware description language (HDL) program for implementing a counter of part (b). You are to utilize ATF750CL PLD programming. [6 marks]

THE END

ALL THE BEST FOR THE EXAMINATION