FIJI NATIONAL UNIVERSITY

Final Examination

College	Engineering, Science & Technology
School	Electrical & Electronics Engineering
Programme	Bachelor of Engineering (BENG Year 4)
Semester	I
Year	2017
Unit Code	EEE796
Unit Title	VHDL & Logic Synthesis
Date of Examination	June 10
Time	9.00 am to 12.10 pm
Venue	TBA
Duration	3 Hours *(extra 10 mins allowed to read the paper)*
Maximum Marks	100

Instructions

1. There are two sections A and B. Both the sections are compulsory.
2. Write your answers legibly in the answer booklet.
3. Write your student identification number on each page used.

Section A: Short Answers *(40 Marks)*

1. State what the following acronyms stands for:
   (a) VHDL (1)
   (b) CPLD (1)
   (c) FPGA (1)
2. How are FPGAs different from CPLDs? (2)
3. Say that s1 to s4 are four VHDL signals. Based on the assignments below, list which synthesizable predefined data types each of these signals can belong to.
   (a) `s1 <= '0';` (1)
   (b) `s2 <= 'Z';` (1)
   (c) `s3 <= TRUE;` (1)
   (d) `s4 <= "01000";` (1)
4. List two synthesizable types defined in the package `standard`. (2)
5. List two synthesizable types defined in the package `std_logic_1164`. (2)
6. Outline the differences between a SIGNAL and a VARIABLE object in VHDL in terms of the following:
   (a) Where a SIGNAL or VARIABLE can be declared (2)
   (b) How is a SIGNAL and VARIABLE updated (2)
   (c) The assignment operator used for SIGNAL and VARIABLE (2)
7. Say that a(7:0) = "00110011" and b(3:0) = "1111". Determine the values produced by the assignments below.
   (a) `a(7 DOWNTO 4) NAND "0111"` (1)
   (b) `a(7 DOWNTO 4) XOR NOT b` (1)
8. For the integers x = 65 and y = 7, calculate:
   (a) `x REM y` (1)
   (b) `x MOD y` (1)
   (c) `ABS(-y)` (1)
9. For x = "110010", of type BIT_VECTOR(5 DOWNTO 0), determine the values of the shift operations below.
   (a) `x SLL 3` (1)
   (b) `x SRA 2` (1)

(c) `x ROL 1` (1)

10. Outline the main difference between FUNCTION and PROCEDURE in VHDL. (2)

11. What is the difference between functional and timing simulation of a VHDL design? (2)

12. What is the main difference between CASE and SELECT statements in VHDL? (1)

13. Write the VHDL code for the circuit shown in Figure 1. (Note: Write concurrent code and use only logical operators) (8)

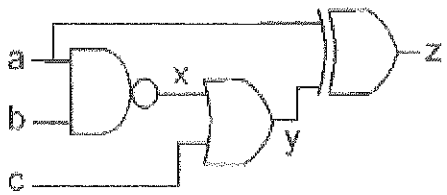


Figure 1: Simple combinational circuit

Section B: Design *(60 Marks)*

1. Using VHDL, design a multiplexer as shown in Figure 2. Use the concurrent statement SELECT and industry standard data types. Also use a GENERIC declaration to set the number of bits N to 8. (10)

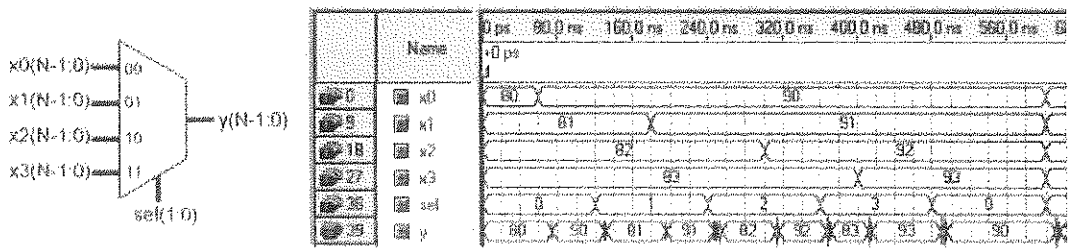


Figure 2: 4 by N multiplexer and simulation results

2. Figure 3 shows, on the left, a diagram for a regular binary 0-to-9 counter. Write a VHDL code to design this circuit. Use the sequential statement PROCESS to design this circuit. (10)

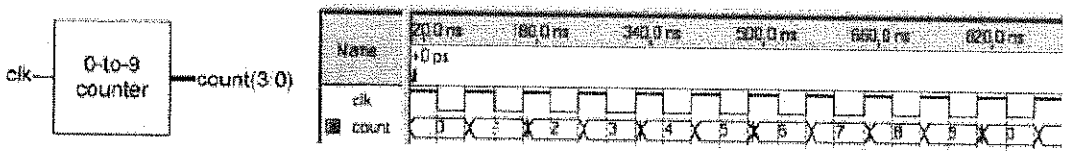
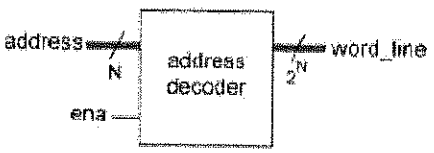


Figure 3: Counter (with simulation results)

3. Design a generic address decoder shown in Figure 4. Use only industry standard ports and use the concurrent statement GENERATE. Use a GENERIC declaration to set the number of bits N to 3. (10)



ena	address	word_line
0	XX	1111
1	00	1110
	01	1101
	10	1011
	11	0111

Figure 4: N bit address decoder

4. Adders are combinational circuits. The simplest multi-bit architecture, shown in Figure 5, is called carry-ripple adder. Each individual cell is called full-adder (FA). Write a VHDL code from which this adder can be inferred. Employ sequential code and enter the number of bits (stages) as a generic parameter, so the code can be easily adjusted to any adder size. Assume that the adder is unsigned. (10)

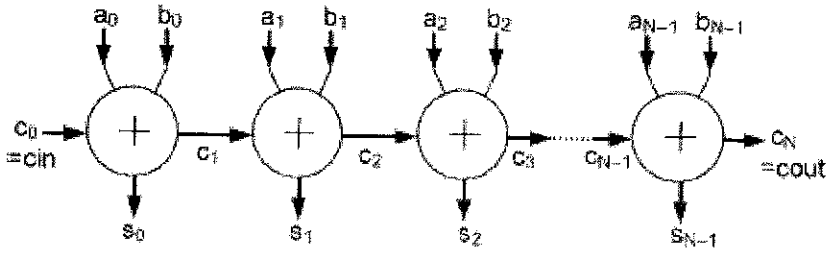


Figure 5: Carry ripple adder

5. Figure 6 shows the schematic of a simple 2 to 1 multiplexer. Model this multiplexer in VHDL using structural/hierarchial modeling concept, i.e., using components. Assume that **and2**, **or2** and **inv** are the primitive components that have been already defined. (10)

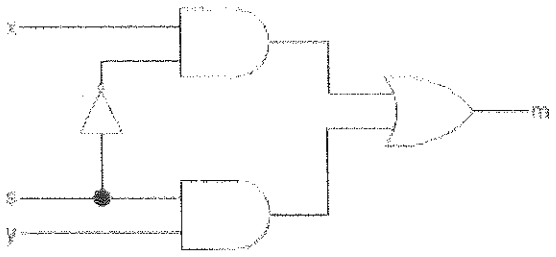


Figure 6: 2-to-1 multiplexer schematic

6. Figure 7 shows a shift register, which consists of a string of serially connected D Flip Flops. The input is din and the output is either q0 to q3 or just dout, depending on the application. For example, the former can be used to convert data from serial to parallel form, while the latter can be used to implement a delay line. Design this circuit using VHDL. The number of stages should be GENERIC. Use sequential IF ELSE statements. (10)

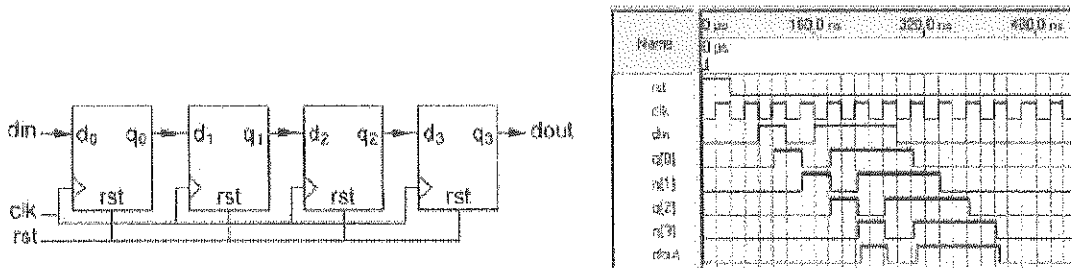


Figure 7: Shift register (with simulation results)

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