FIJI NATIONAL UNIVERSITY

COLLEGE: COLLEGE OF ENGINEERING, SCIENCE & TECHNOLOGY (CEST)

SCHOOL: SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

PROGRAMME: CERTIFICATE IV IN ELECTRONICS ENGINEERING

UNIT CODE: EEE412

TITLE: DIGITAL ELECTRONICS 1A

FINAL EXAMINATION – PENSTER 3, 2017

TIME: 2 HOURS & 10 MINUTES
ROOM: AS PER TIMETABLE

INSTRUCTIONS TO STUDENTS

1. You are allowed **10 minutes** extra **reading time** during which you are **NOT** to write.
2. Begin each SECTION on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each attached sheet.
4. Insert all written foolscaps, graph paper, drawing paper, etc. in their correct sequence and secure with a string.
5. For all sheets of paper on which rough/draft work has been done, cross it through and ATTACH these to your answer scripts.
6. Write clearly the number(s) of the question(s) attempted on the top of each sheet.
7. Use of programmable calculator(s) is prohibited.
8. ANSWER ALL QUESTIONS
9. Show all working where necessary.
10. ALWAYS CHECK YOUR WORK BEFORE YOU LEAVE THE EXAM ROOM.

Section A Attempt all the questions [40 marks]

1. Determine the binary ASCII codes that are entered from the computer's keyboard when the following basic program statement is typed in. Also express each code in hexadecimal.
   20 INT **(3 marks)**

2. Flip-flops are synchronous bistable devices, also known as bistable multivibrators. The S-R, J-K and D inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. Define the following:
   a) Propagation delay time **(1 mark)**
   b) Hold time **(1 mark)**
   c) Pulse width **(1 mark)**

3. The complement of the union of two sets is equal to the intersection of their complements and the complement of the intersection of two sets is equal to the union of their complements. These are called De Morgan's laws. Apply DeMorgan's theorems to the following expression:

   a) $\overline{(ABC+DEF)}$ **(2 marks)**

   b) $\overline{(\bar{A}+B)+CD}$ **(3 marks)**

4. Convert the following decimal number to binary:
   a) 82 **(2 marks)**
   b) 294 **(2 marks)**

5. Logic gates can be constructed by using simple switches, relays, vacuum tubes, transistors, IC's and diodes. Draw the following circuit using switches.

   a) OR **(2 marks)**
   b) AND **(2 marks)**

6. With the aid of diagrams explain the difference between analogue and digital techniques and give one application of each. **(6 marks)**

7. Convert the following decimal numbers to BCD:

a) .170 **(2marks)**
b) .2469 **(2marks)**

8. Convert the following Gray code to binary.

a) 01101 **(2marks)**
b) 10101111 **(2marks)**

9. Differentiate between a counter and a shift register? **(3marks)**

10. Convert the following Boolean expression into standard POS form:

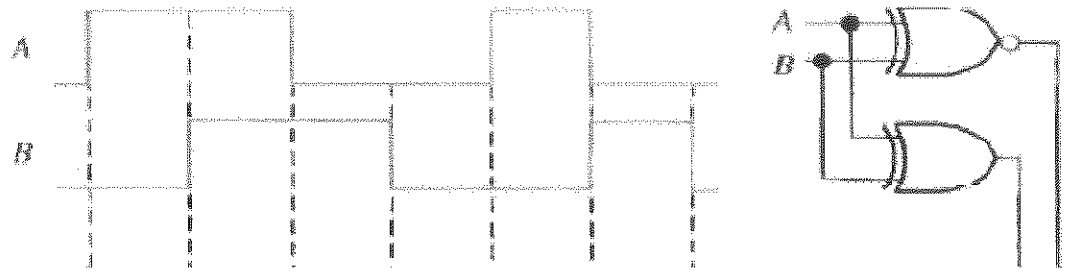
$(A+\bar{B}+C)\,(\bar{B}+C+\bar{D})\,(A+\bar{B}+\bar{C}+D)$ **(4 marks)**

Section B **Attempt all the questions** **[60 marks]**

1. The basic building block of any digital circuit is a logic gate. Determine the logic symbol, boolean expression and the truth table for the following two input logic function:

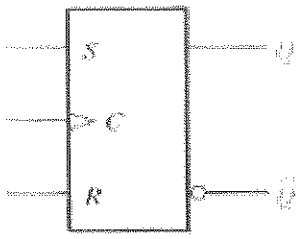
   a) AND gate **(6 marks)**
   b) OR gate **(6 marks)**

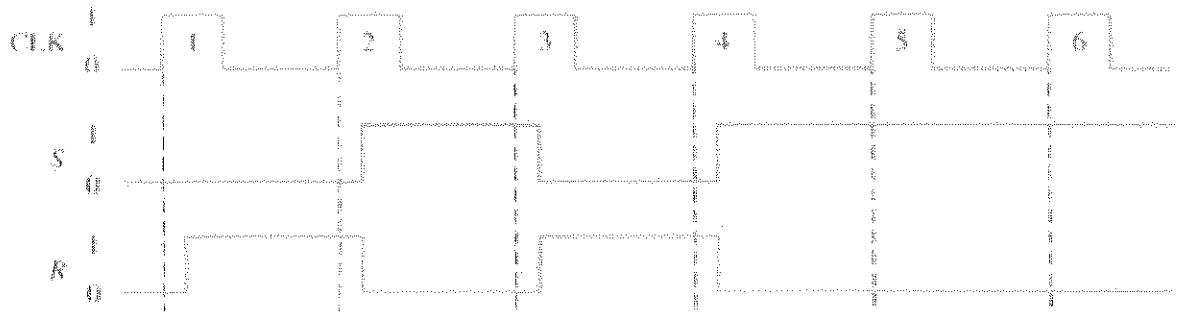
2. Determine the output waveforms for the XOR gate and for the XNOR gate, given the input waveforms, A and B, as in figure below.



(6 marks)

3. Determine the Q and $\bar{Q}$ output waveforms of the flip-flop shown below, for the S, R, and CLK inputs in figure below. Assume that the positive edge-triggered flip-flop is initially RESET.





(5 marks)

4. Draw and explain serial in / serial out shift registers. **(6 marks)**

5. Convert the following Boolean expression into standard SOP form:

$A\bar{B}C + \bar{A}\,\bar{B} + AB\bar{C}\,D$ **(3 marks)**

6. Consider the Boolean expression:

$A.\bar{B}.\bar{C}.\bar{D} + \bar{A}.B.\bar{C}.D + \bar{A}.\bar{B}.\bar{C}.D + \bar{A}.\bar{B}.C.D + \bar{A}.B.C.D + A.\bar{B}.\bar{C}.D = Y$

a) Draw the four variable Karnaugh map and eliminate variables by looping. **(8 marks)**
b) Write the simplified Boolean expression. **(2 marks)**

7. Draw a 2–bit synchronous binary counter and explain its operation. **(7 marks)**

8. Using the given data sheet, determine it's:
a) High level noise margin **(3 marks)**
b) Low level noise margin **(3 marks)**
c) Supply voltage **(1 mark)**
d) Power dissipation **(4 marks)**

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			6.1	9.2	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			10.3	15.5	mA	Max	V_O = LOW

AC Electrical Characteristics

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = −55°C to +125°C, V_{CC} = +5.0V, C_L = 50 pF		T_A = 0°C to +70°C, V_{CC} = +5.0V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	4.2	5.6	3.0	7.5	3.0	6.6	ns
t_{PHL}	A_n, B_n to O_n	3.0	4.0	5.3	2.5	7.5	3.0	6.3	

Decimal	Octal	Hex	Binary	Value	
000	000	000	00000000	NUL	(Null char.)
001	001	001	00000001	SOH	(Start of Header)
002	002	002	00000010	STX	(Start of Text)
003	003	003	00000011	ETX	(End of Text)
004	004	004	00000100	EOT	(End of Transmission)
005	005	005	00000101	ENQ	(Enquiry)
006	006	006	00000110	ACK	(Acknowledgment)
007	007	007	00000111	BEL	(Bell)
008	010	008	00001000	BS	(Backspace)
009	011	009	00001001	HT	(Horizontal Tab)
010	012	00A	00001010	LF	(Line Feed)
011	013	00B	00001011	VT	(Vertical Tab)
012	014	00C	00001100	FF	(Form Feed)
013	015	00D	00001101	CR	(Carriage Return)
014	016	00E	00001110	SO	(Shift Out)
015	017	00F	00001111	SI	(Shift In)
016	020	010	00010000	DLE	(Data Link Escape)
017	021	011	00010001	DC1	(XON) (Device Control 1)
018	022	012	00010010	DC2	(Device Control 2)
019	023	013	00010011	DC3	(XOFF)(Device Control 3)
020	024	014	00010100	DC4	(Device Control 4)
021	025	015	00010101	NAK	(Negative Acknowledgement)
022	026	016	00010110	SYN	(Synchronous Idle)
023	027	017	00010111	ETB	(End of Trans. Block)
024	030	018	00011000	CAN	(Cancel)
025	031	019	00011001	EM	(End of Medium)
026	032	01A	00011010	SUB	(Substitute)
027	033	01B	00011011	ESC	(Escape)
028	034	01C	00011100	FS	(File Separator)
029	035	01D	00011101	GS	(Group Separator)
030	036	01E	00011110	RS	(Request to Send)(Record Separator)
031	037	01F	00011111	US	(Unit Separator)
032	040	020	00100000	SP	(Space)
033	041	021	00100001	!	(exclamation mark)
034	042	022	00100010	"	(double quote)
035	043	023	00100011	#	(number sign)
036	044	024	00100100	$	(dollar sign)
037	045	025	00100101	%	(percent)
038	046	026	00100110	&	(ampersand)
039	047	027	00100111	'	(single quote)
040	050	028	00101000	(	(left/opening parenthesis)
041	051	029	00101001	)	(right/closing parenthesis)
042	052	02A	00101010	*	(asterisk)
043	053	02B	00101011	+	(plus)
044	054	02C	00101100	,	(comma)
045	055	02D	00101101	-	(minus or dash)
046	056	02E	00101110	.	(dot)
047	057	02F	00101111	/	(forward slash)
048	060	030	00110000	0	
049	061	031	00110001	1	
050	062	032	00110010	2	
051	063	033	00110011	3	
052	064	034	00110100	4	
053	065	035	00110101	5	
054	066	036	00110110	6	
055	067	037	00110111	7	
056	070	038	00111000	8	
057	071	039	00111001	9	
058	072	03A	00111010	:	(colon)
059	073	03B	00111011	;	(semi-colon)
060	074	03C	00111100	<	(less than)
061	075	03D	00111101	=	(equal sign)
062	076	03E	00111110	>	(greater than)

063	077	03F	00111111	?	(question mark)
064	100	040	01000000	@	(AT symbol)
065	101	041	01000001	A	
066	102	042	01000010	B	
067	103	043	01000011	C	
068	104	044	01000100	D	
069	105	045	01000101	E	
070	106	046	01000110	F	
071	107	047	01000111	G	
072	110	048	01001000	H	
073	111	049	01001001	I	
074	112	04A	01001010	J	
075	113	04B	01001011	K	
076	114	04C	01001100	L	
077	115	04D	01001101	M	
078	116	04E	01001110	N	
079	117	04F	01001111	O	
080	120	050	01010000	P	
081	121	051	01010001	Q	
082	122	052	01010010	R	
083	123	053	01010011	S	
084	124	054	01010100	T	
085	125	055	01010101	U	
086	126	056	01010110	V	
087	127	057	01010111	W	
088	130	058	01011000	X	
089	131	059	01011001	Y	
090	132	05A	01011010	Z	
091	133	05B	01011011	[	(left/opening bracket)
092	134	05C	01011100	\	(back slash)
093	135	05D	01011101	]	(right/closing bracket)
094	136	05E	01011110	^	(caret/circumflex)
095	137	05F	01011111	_	(underscore)
096	140	060	01100000	`	
097	141	061	01100001	a	
098	142	062	01100010	b	
099	143	063	01100011	c	
100	144	064	01100100	d	
101	145	065	01100101	e	
102	146	066	01100110	f	
103	147	067	01100111	g	
104	150	068	01101000	h	
105	151	069	01101001	i	
106	152	06A	01101010	j	
107	153	06B	01101011	k	
108	154	06C	01101100	l	
109	155	06D	01101101	m	
110	156	06E	01101110	n	
111	157	06F	01101111	o	
112	160	070	01110000	p	
113	161	071	01110001	q	
114	162	072	01110010	r	
115	163	073	01110011	s	
116	164	074	01110100	t	
117	165	075	01110101	u	
118	166	076	01110110	v	
119	167	077	01110111	w	
120	170	078	01111000	x	
121	171	079	01111001	y	
122	172	07A	01111010	z	
123	173	07B	01111011	{	(left/opening brace)
124	174	07C	01111100	|	(vertical bar)
125	175	07D	01111101	}	(right/closing brace)
126	176	07E	01111110	~	(tilde)
127	177	07F	01111111	DEL	(delete)

----------THE END----------