

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

ADVANCED DIPLOMA IN ENGINEERING (ELECTRICAL & ELECTRONIC)

EEE604 – ELECTRO TECHNOLOGY(ELECTRONIC)

SPECIAL EXAM – TRIMESTER-3, 2016

DAY/DATE: 1/12/2016 TIME : 2:00 – 5.10PM

ROOM: TBA

INSTRUCTION TO STUDENT

1. You are allowed 10 minutes extra reading time during which you are NOT to write.
2. **Begin** each Question on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each answer & attached sheet.
4. Insert all written foolscaps, graph paper etc. in their correct sequence and secure with a string.
5. For all sheets of paper on which rough/draft work has been done, cross it through and you must attach all of them to your answer scripts.
6. Write clearly the number(s) of the question(s) attempted on the top of each sheet.
7. Tables & formula on the Appendix.
8. **SECTION A. -- MULTIPLE CHOICE & SHORT ANSWER**
SECTION B. – SELECT TWO(2) QUESTION
SECTION C. – PICK ANY TWO(2) QUESTION

SECTION - A: - Multiple Choice [15marks]

Choose only ONE correct answer from the choice given and use the Answer Sheet provided in your Answer Booklet.

- (1) For the CE Amplifier configuration, BJT Transistors is switched on by the ..?
- (a) The current flow through it from biasing voltage.
 - (b) Biasing voltage is fixed by the potential divider connected to the base.
 - (c) Reverse breakdown voltage
 - (d) The current through it results from both kinds of charge carriers
- (2) In a Sequential Logic Circuits, synchronous system does
- (a) Create two terminal device used to vary the current in the circuit
 - (b) Affect the output to propagate throughout the system.
 - (c) Sampled output at a definite instant time.
 - (d) Create two terminal device used for storing voltage.
- (3) The FET(field effect transistors) is classified as
- (a) Gate biasing current device.
 - (b) Collector biasing voltage device.
 - (c) Current-controlled device.
 - (d) Voltage-controlled device.
- (4) Select one characteristics of a Synchronous system?
- (a) Clock signals to be distributed to few flip flops.
 - (b) Types of clock for controlling the system.
 - (c) Clock signals to be distributed to every flip flops
 - (d) Clock signals are a high frequency signal.
- (5) Identify the correct statement which defines Asynchronous System.
- (a) Two terminal device used to vary the current in the circuit
 - (b) Circuit responds to changes at the input at any time.
 - (c) A two terminal device that resist the flow of current.
 - (d) Do have common clock.

- (6) Why do Class A Amplifiers are not used for Power design?
- (a) Low distortion and inefficient.
 - (b) Tends to generate a lot heat energy.
 - (c) High theoretical efficiency of $\pi/4$
 - (d) Used for signal conditioning
- (7) Select the main characteristics of the counters?
- (a) All memory elements are triggered simultaneously
 - (b) Remembers its past states
 - (c) Limits number of flip-flops used
 - (d) Determine the number of states and sequence.
- (8) What is the purpose of *Oscillator* in an electronic system?
- (a) Create dc from ac voltage
 - (b) Blocks ac voltages and allow dc voltage
 - (c) Generator of sine-wave signal
 - (d) Produce amplification
- (9) Determine the filter model type which uses *Anti-Aliasing Filter in Data converter* applications?
- (a) Tschebyscheff High Pass Filters.
 - (b) Butterworth High Pass Filters
 - (c) Tschebyscheff Low Pass Filters
 - (d) Butterworth Low Pass Filters
- (10) In Digital Circuit designing, which of the following device you will need to display the number you pressed on the keypad after releasing your finger?
- (a) Decoder
 - (b) Encoder.
 - (c) Latching circuit.
 - (d) Multiplexor

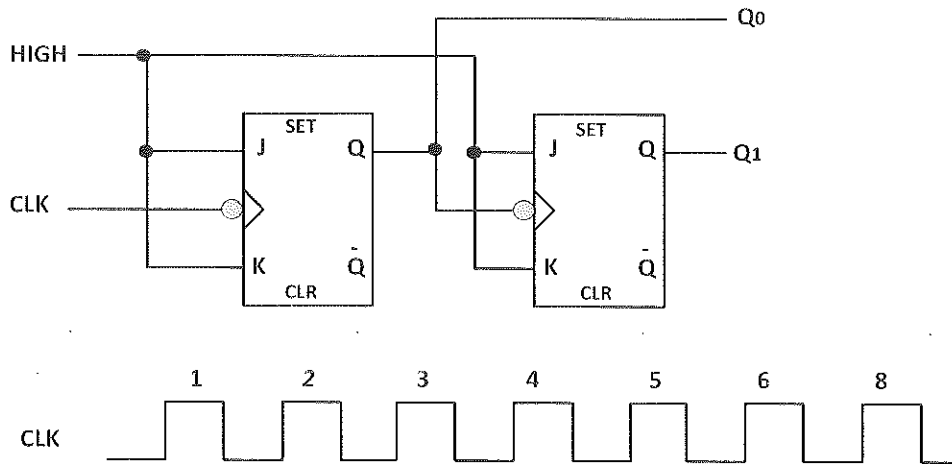
- (11) In Oscillators designing, two things which must be achieved before the oscillator can oscillate?
- (a) Biasing voltage and loop gain
 - (b) Phase shift and high gain.
 - (c) Low gain and phase angle.
 - (d) Unity loop gain and phase shift
- (12) Identify the best filter types used in *System Power Supplies*?
- (a) High Pass Filters
 - (b) Low Pass Filters
 - (c) Band stop filters.
 - (d) Band rejection filters
- (13) Which Amplifier type which generates PWM output for its train pulses having width that are proportional to the level of the amplifier's input?
- (a) Class D.
 - (b) Class B.
 - (c) Class C.
 - (d) Class A.
- (14) Approximately, what is the efficiency of a Class B amplifier?
- (a) 50%
 - (b) 78%
 - (c) 90%
 - (d) 25%
- (15) What are the passive components in the Clapp Oscillator configuration
- (a) Capacitors and Resistors
 - (b) Resistors and Inductors
 - (c) Inductors and Capacitors
 - (d) Capacitors and diodes.

SECTION - A:

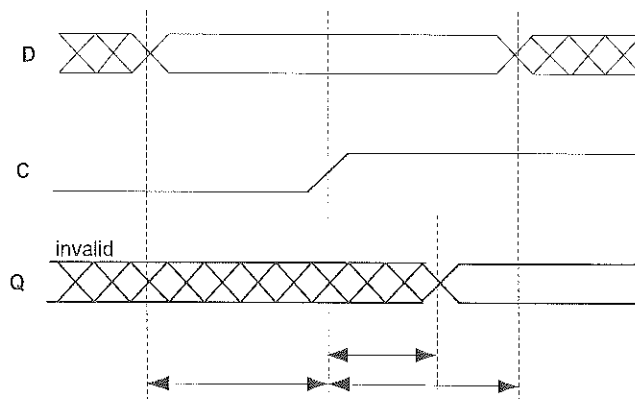
SHORT ANSWERS

(5 marks)

1. Draw the Output Timing Diagram for the Asynchronous Ripple Counters below. [3 marks]



2. Label the timing characteristics of the edge-triggered register. [2 marks]



SECTION - B: Optional Section Answer any 2 Question from this section.

Question 1 FET Amplifier Application

An NMOS inverter in the figure -1 below has the following parameters: $V_{T1} = V_{T2} = 2\text{v}$, $\beta_1 = 0.45 \times 10^{-3}$, $\beta_2 = 0.045 \times 10^{-3}$ and $V_{DD} = 12\text{v}$.

Determine the *high* and *low* output voltage.

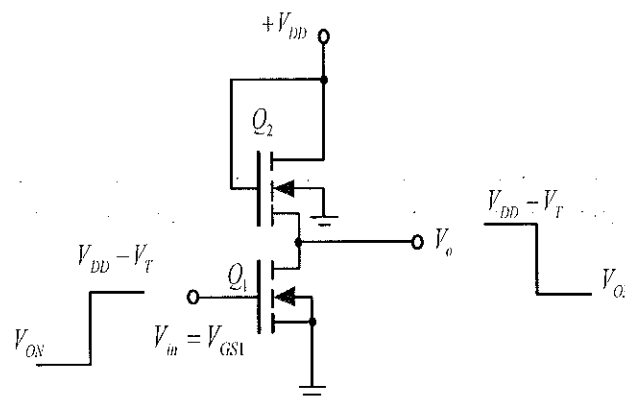


Fig.1 - NMOS Inverter Switch

[20 marks]

Question – 2: 2nd Order LP Filter Design

Using the coefficient table attached at the back, design and draw an Active Second Order unity-gain Tschebyscheff Low-pass Filter with a cut-off frequency of 7kHz and a 3-dB pass-band ripple with $C1 = 22\text{nF}$.

[20 marks]

Question - 3

Oscillator Design

The gain of a certain oscillator system in fig.2 below as a function of frequency is $A(j\omega) = -16 \times 10^6 / j\omega$. A feedback path connected around it has $\beta(j\omega) = 10^3 / (2 \times 10^3 + j\omega)^2$.

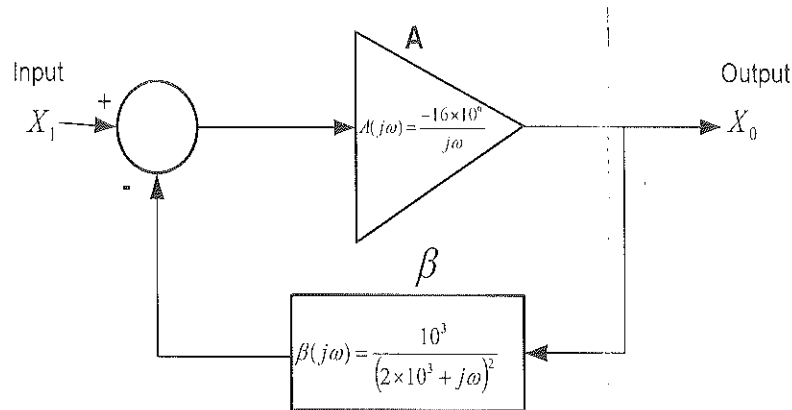


Fig.2 - Oscillator system

- (a). Use Rectangular or Polar form to determine if the system will oscillate. (16 marks)
(b). Determine if your oscillator design will work, what will be the frequency that your oscillator will operate? (4 mark)

[20 marks]

Question - 4 Multiplexer & Registers Design

- (a) In the address decoding circuit in figure-3 below for a 4 x 8-bit shift register with an address decoder.
- Write down the Truth table for the system.
 - Write down the address combination which will select the following register C, A, D, B?
 - How many output will the five input decoder have?
 - Referring to part (iii), write down the truth table

[10 marks]

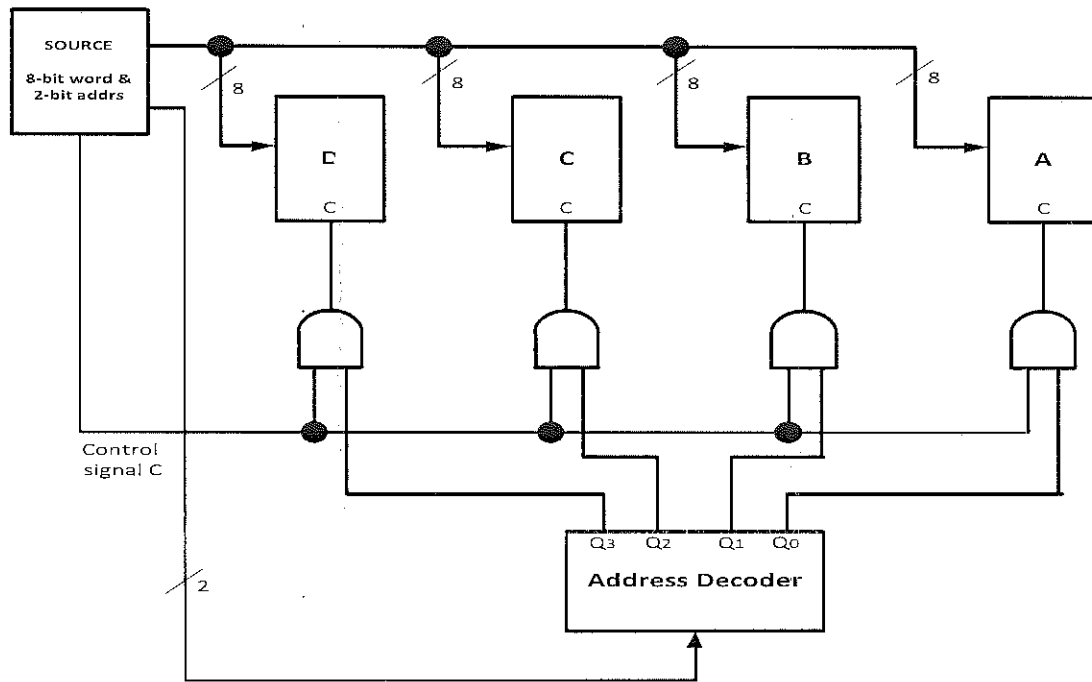


Figure-3: 2-Line Address decoder.

- (b) Design and draw a Serial-In Parallel-out Shift Register using D type Flip flop that will do the following:-
- Receive the following serial data 101101001 in its input.
 - The clock circuit is common, to trigger in its trailing edge.
 - Draw its Timing Diagram for the next 10 clock pulse.
 - Explain the main effect of using Asynchronize clock circuit

[10 marks]

[20 marks]

SECTION - C: Answer any 2 Question from this section.

Question - 1 Series-Fed Class-A Amplifier

Referring to figure 4 below, an input voltage (V_{in}) in a base current of 10mA peak produces the characteristics shown in fig. 4(b) for a series-fed Class A amplifier. Calculate the following:-

- (i) Input Power (4 marks)
- (ii) Output Power (4 marks)
- (iii) Efficiency of Amp (4 marks)
- (iv) Power dissipated by the transistor (4 marks)
- (v) Identify advantages and disadvantages of negative feedback. (4 marks)

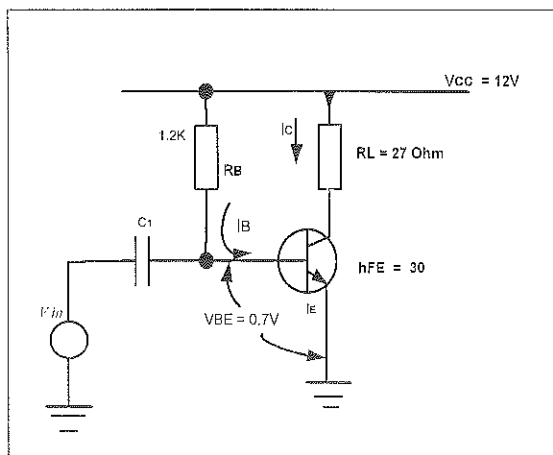


Fig.4a – Series-fed Class A Amplifier

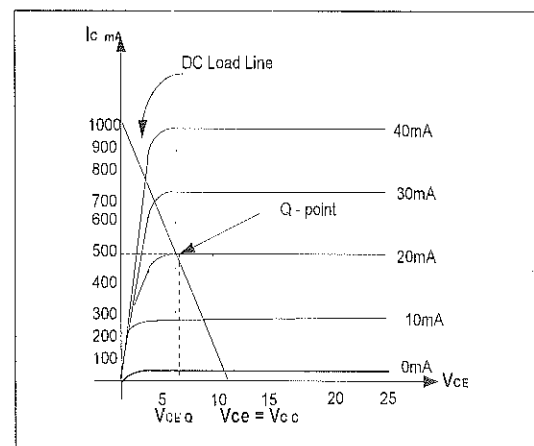


Fig.4b -- Series-fed Class A characteristics graph

[20 Marks]

Question 2:

Class C Power Amplifier

Fig.5 below shows a class C Power Amplifier with base bias voltage of -6V and $V_{CC} = 30\text{V}$. It is determined that a peak input voltage of 8.6V at 1MHz is required to drive the transistor to its saturation current of 1.7A

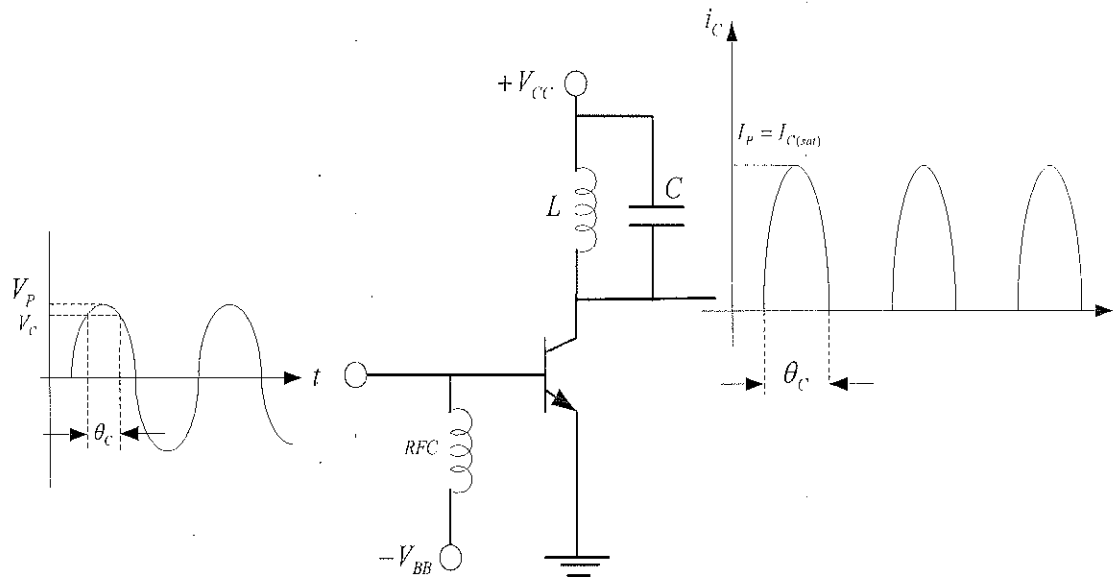


Fig.5 – Class C Power Amplifier

. Determine the following:-

- Amplifier's conduction angle. (5 marks)
- Amplifier's output power at 1MHz . (5 marks)
- Amplifier's efficiency. (4 marks)
- If the LC tank circuit having $C = 470\text{pF}$ is connected in the collector circuit, find the inductance necessary to tune the amplifier. (6 marks)

(6 marks)

[20 marks]

Question 3: General Amplifier's Characteristics

- (a) Clearly state all advantages and disadvantages of positive feedback. [3 marks]
- (b) Explain with aid of diagram the effect of increasing V_{DS} in N-Channel JFET, while gate is shorted to source, $V_{GS} = 0$. [7 marks]
- (c) Find the output voltage of the amplifier shown in figure 6 below, assuming that $r_s = 22\Omega$. [10 marks]

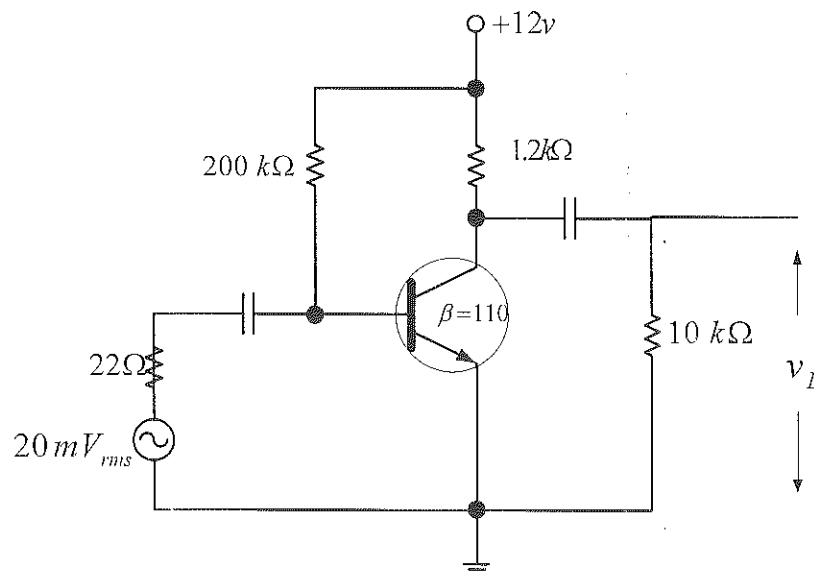


Fig. 6 - Common Emitter BJT amplifier

[20 marks]

Question - 4

Digital System Design & OP amps

- (a) Figure 7 below shows a 4-bit synchronous shift register with Q_D output connected back to the DA input via an inverter. Assuming the initial state of the register is 0101.

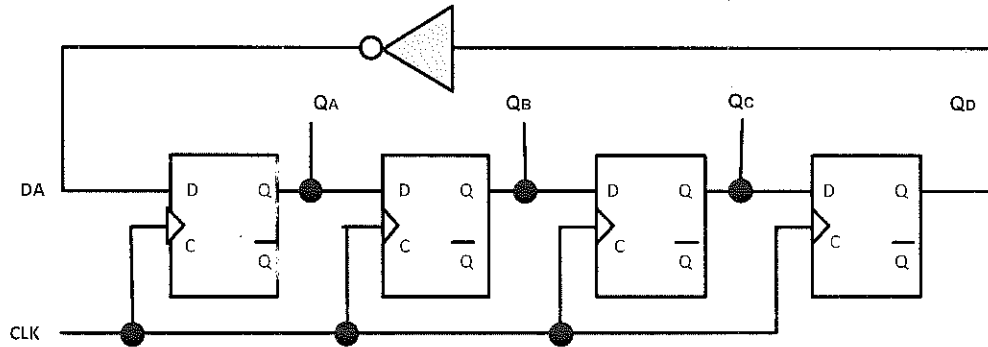


Figure-7: 4-bit Shift Register.

Give a brief account of how the above system works and produce the timing diagram for the output Q_A to Q_D for the next 10 clock pulses, before the output are repeated. [10 marks]

- (b) In a non-inverting circuit in figure-8 below, the input resistance r_{in} of the op amp on its own is $110k\Omega$ and the voltage gain A_v of the Op amp is 210,000. [6 marks]

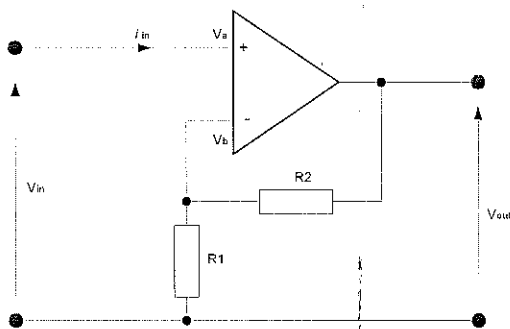


Fig.8 - Non- Inverting Amplifier

Calculate the overall gain G , and the input resistance R_{in} of the circuit above when:-

- (i) $R_1 = 1K\Omega$ and $R_2 = 40K\Omega$.
- (ii) $R_2 = 0$
- (iii) $R_1 = 0K\Omega$ and $R_2 = 40K\Omega$.

- (c) Briefly explain the applications, advantages & disadvantages of class-B amplifier system.

[4 marks]

[20 marks]

-----THE END -----

Appendix 1

Formulas

$$1. \quad \frac{1}{2}\beta_2[(V_{DD} - V_{ON}) - V_T]^2, \quad \beta_1[(V_{DD} - 2V_T)V_{ON} - 0.5^2 V_{ON}]$$

$$2. \quad A_i = \frac{hfe}{1 + hoe \cdot R_L} \quad A_p = 6\left(\frac{D}{\lambda}\right)^2$$

$$3. \quad C_2 = C_1 \frac{4b_1}{a_1^2} \quad P_Q = \left(\frac{2}{\pi^2} \times \frac{V_{CC}^2}{R_L}\right) / 2$$

$$4. \quad K_O K_D = \frac{33.6 f_O}{V_C} \quad X_1 = \frac{a_1 C_2 \pm \sqrt{(a_1 C_2)^2 - 4b_1 C_1 C_2}}{4\pi f_c C_1 C_2}$$

$$5. \quad X_C = \frac{1}{2\pi f C} \quad X_L = 2\pi f L \quad P_{R(DC)} = V_{CC} \cdot \left(\frac{2}{\pi} \cdot \frac{V_{CC}}{R_L}\right)$$

$$6. \quad f = \frac{1}{2\pi \sqrt{6RC}} \quad I_D = \beta V_{DS} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right)$$

$$7. \quad A_v = \frac{V_O}{V_i} = \left[hre - \frac{hie}{hfe} \left(\frac{1 + hoe \cdot R_L'}{R_L'} \right) \right]^{-1} \quad I_D = \frac{\beta(V_{GS} - V_T)^2 (1 + \lambda V_{DS})}{2}$$

$$8. \quad I_B = \frac{V_{CC} - 0.7V}{R_B}, \quad I_C = h_{FE} \cdot I_B, \quad V_{ce} = V_{CC} - I_C R_L$$

$$9. \quad I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2, \quad \beta_1[(V_{DD} - 2V_T)V_{ON} - 0.5^2 V_{ON}]$$

$$10. \quad f_H = \pm \frac{8f_O}{V_C}, \quad V_{DS} = V_{DD} - I_D R_D$$

Appendix 2

Filter Coefficients

SECOND-ORDER	BESSEL	BUTTERWORTH	3-dB TSCHEBYSCHIEFF
a_1	1.3617	1.4142	1.065
b_1	0.618	1	1.9305
Q	0.58	0.71	1.3
R_1/R_2	0.268	0.568	0.234

Second-Order Filter Coefficients

Tschebyscheff Coefficients

n	l	a_l	b_l	$k_l = \frac{\omega_c l}{\omega_c}$	Q _l
1	1	1.0000	0.0000	1.000	—
2	1	1.3614	1.3827	1.000	0.66
3	1	1.8638	0.0000	0.537	—
	2	0.0640	1.1931	1.335	1.71
4	1	2.6282	3.4341	0.536	0.71
	2	0.3648	1.1509	1.419	2.84
5	1	3.9235	0.0000	0.340	—
	2	1.3025	2.3534	0.361	1.18
	3	0.0290	1.0833	1.460	4.54
6	1	5.9645	6.6797	0.368	0.68
	2	0.7528	1.8573	1.078	1.81
	3	0.1589	1.0711	1.495	6.51
7	1	9.0211	0.0000	0.249	—
	2	1.6729	4.1756	0.645	1.09
	3	0.4381	1.5679	1.208	2.58
	4	0.1156	1.0443	1.517	8.64
8	1	13.9117	11.960	0.276	0.68
	2	1.0699	2.9355	0.844	1.61
	3	0.3439	1.4206	1.284	3.47
	4	0.0895	1.0407	1.521	11.53
9	1	19.1318	0.0000	0.195	—
	2	2.4283	6.6307	0.506	1.06
	3	0.6839	2.2938	0.969	2.21
	4	0.2559	1.3133	1.344	4.48
	5	0.0895	1.0072	1.532	14.58
10	1	26.3648	18.369	0.222	0.67
	2	1.2582	4.2453	0.689	1.53
	3	0.4822	1.8440	1.091	2.89
	4	0.1994	1.2520	1.381	5.61
	5	0.0583	1.0063	1.533	17.99