FNU FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE AND TECHNOLOGY

School of Electrical & Electronics Engineering

Trade Diploma in Electronics Engineering

EEE476 – Analog Electronics I

FINAL EXAMINATION

Trimester 3, 2016

Date: As per Exam Time Table

Time: As per Exam Time Table

Venue: As per Exam Timetable

Instructions to Students

1. You are allowed an extra ten (10) minutes of reading time during which you are NOT allowed to write.
2. Attempt ALL questions in this examination booklet
3. Write your answers in the answer booklet provided.
4. Write your Student ID number on each page used.
5. Begin each Section on a fresh page and use both sides of the answer sheet.
6. You may use calculators provided they are non-programmable.
7. Clearly number the questions in your answer paper in their correct sequence and write legibly. Show all working.
8. Attach any extra sheets used to your answer booklet securely with the string provided.

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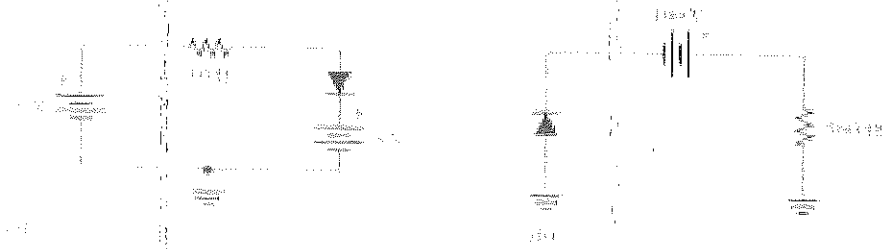
Question 1: Semiconductors/ Diode and application [20 marks]

a) Define each of the terms: **(3 marks)**
   i) Valence band
   ii) Insulators
   iii) Conductors
   iv) Semiconductor

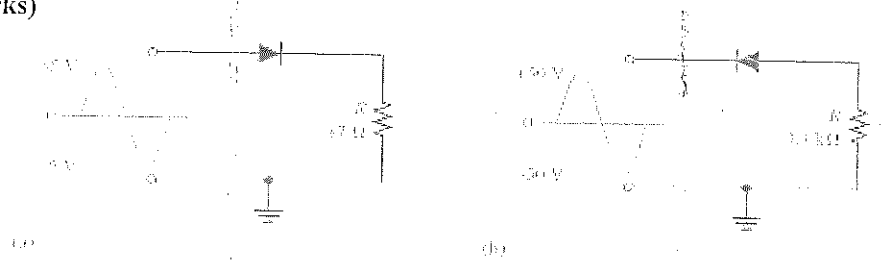
b) Describe how a pn junction is formed. **(3 marks)**

c) Explain why a series resistor is necessary when a diode is forward-biased. **(2 marks)**

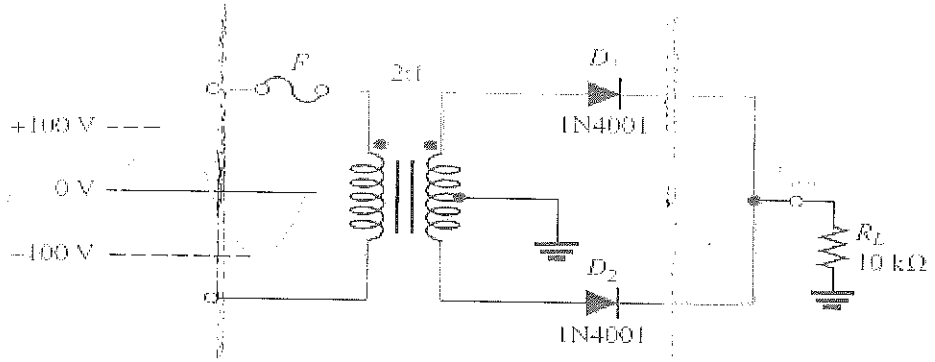
d) Determine whether each silicon diode in Figure below is forward-biased or reverse-biased and find the voltage across each diode. Assuming an ideal diode. **(3 marks)**



e) Draw the output voltage waveform for each circuit in Figure below and include the voltage values. **(2 marks)**



h) For the Figure given below: **(3 marks)**
   i) Show the voltage waveform across each half of the secondary winding and across R_L when a 100 V peak sine wave is applied to the primary winding.
   ii) Find the peak value of the output voltage and the PIV of the diode in the circuit.



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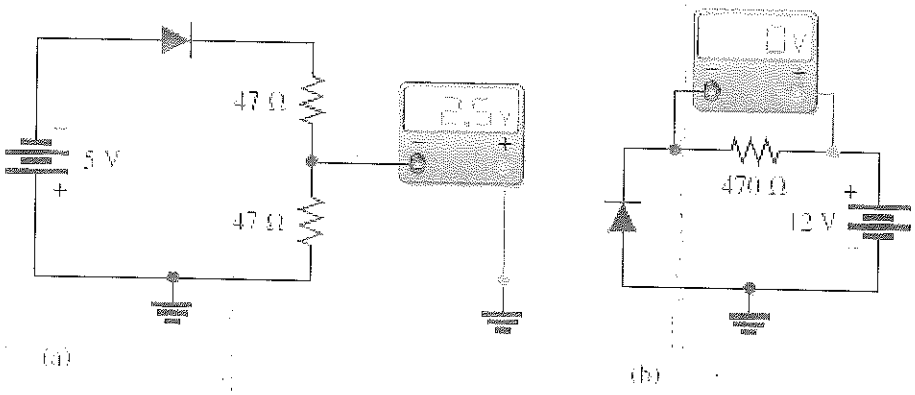
i) Outline what multimeter reading will show when testing a good diode. **(2 marks)**

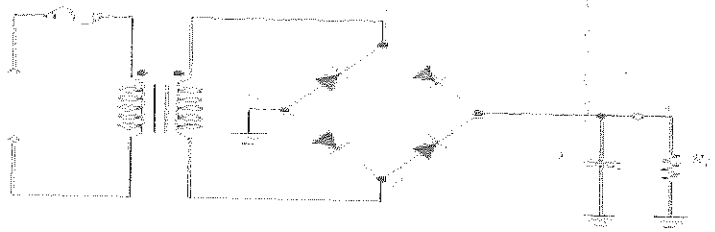
j) Consider the meter indication in the circuit in Figure below and determine whether the diode is functioning properly, or whether it is open or shorted. Assume the ideal model. **(2 marks)**



(a) (b)

Question 2: Power Supplies [20 marks]

a) Determine the peak-to-peak ripple and dc output voltage in Figure below. The transformer has a 50V rms secondary voltage rating and the line voltage has a frequency of 60Hz. Use C= 150μF and RL = 3K ohm. **(5 marks)**



b) What value of filter capacitor is required to produce a 3% ripple factor for a full-wave rectifier having a load resistance of 1.5K ohm. Assume the rectifier produces a peak output of 18V and input frequency is 60 Hz. **(5 marks)**

c) Calculate the peak voltage across each half of a center-tapped transformer used in a full-wave rectifier that has an average output voltage of 130V. **(3 marks)**

d) Draw the block diagram of the Switch mode power supply (SMPS) and outline the function of each block. **(4 marks)**

e) Draw and describe the V-I characteristics of a zener diode and analyze its operation. **(3 marks)**

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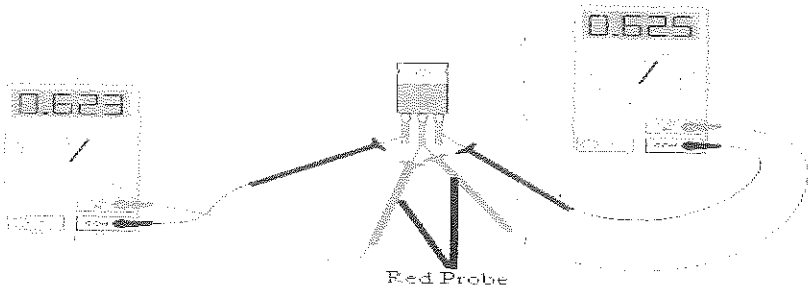
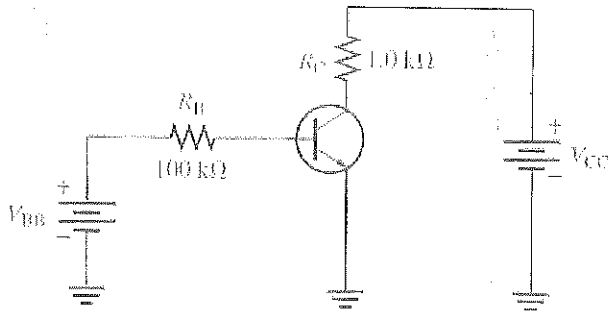
Question 3: BJTs, BJT bias circuits and amplifiers [30 marks]

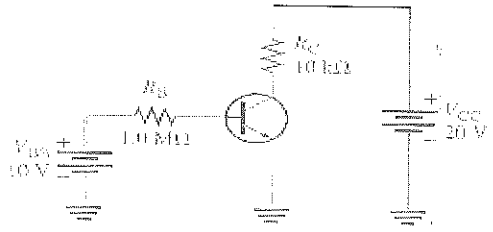
a) Identify the terminals of BJT given below and what type of BJT it is (NPN or PNP). **(2 marks)**



b) A base current of 50μA is applied to the transistor in Figure below and a voltage of 5V is dropped across R_C. Determine β_{DC} of the transistor. **(2 marks)**



c) Determine the DC Q-point in Figure below and draw the DC load line. Find the maximum peak value of base current for linear operation. β_{DC}= 200 **(5 marks)**



d) A certain transistor is to be operated with V_{CE}=10V. If its maximum power rating is 300mW, what is the most collector current that it can handle. **(3 marks)**

e) The LED in Figure below requires 30mA to emit a sufficient level of light. Therefore, the collector current should be approximately 30mA. For the following circuit values, determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. Use double the minimum value of the base current as a safety margin to ensure saturation. V_{CC} = 9V, $V_{CE(sat)}$ = 0.3V, R_C = 220 ohms, R_B = 3.3kohms, β_{DC} = 50 and V_{LED} = 1.6 V. **(4 marks)**

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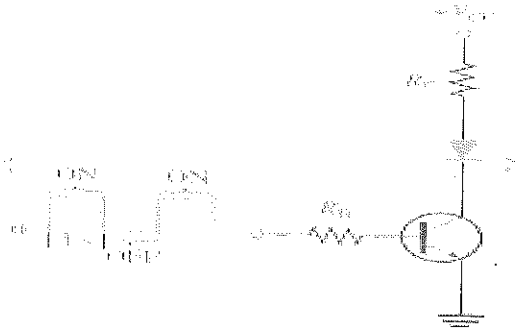
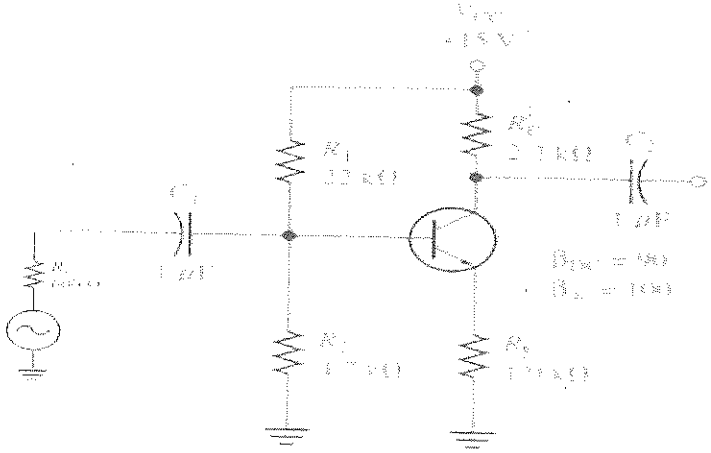
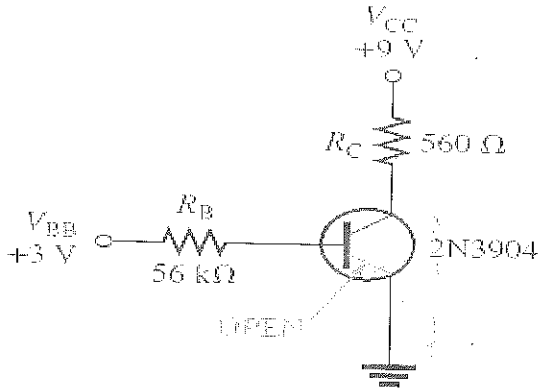


f) For the Figure given below:
   i. Draw the DC analysis circuit and determine V_{CE}. **(4 marks)**
   ii. Draw AC analysis circuits for the amplifier given below and determine output voltage. **(5 marks)**



g) List down the 2 types of transistor biasing methods and outline which one is commonly used and why? **(3 marks)**

h) What is the most likely symptom resulting from emitter internally open in Figure below. **(2 marks)**



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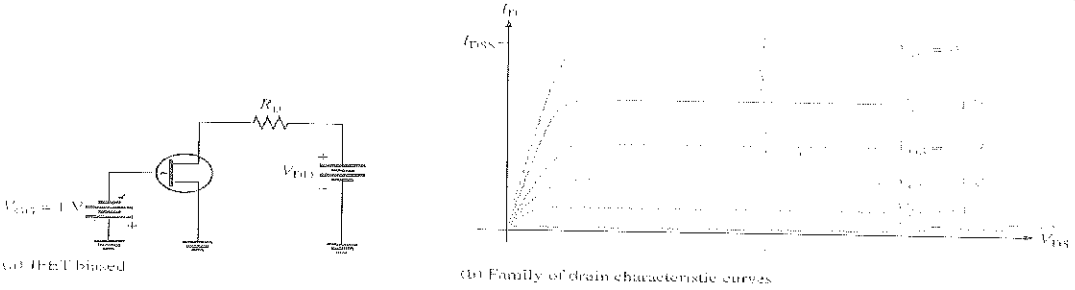
Question 4: FETs [15 marks]

a) Draw the basic circuit and describe the operation of JFET. **(4 marks)**

b) What three areas are the drain characteristics of a JFET (VGS = 0) divided into? **(2 marks)**

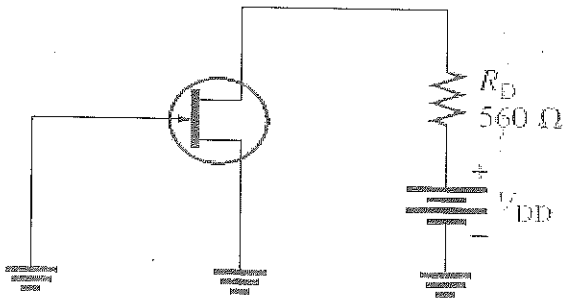
c) For JFET drain characteristics, define Pinch-off voltage. **(2 marks)**

d) In the Figure below, label Vp (Pinch-off voltage) for VGS =0V and determine its value. **(3 marks)**



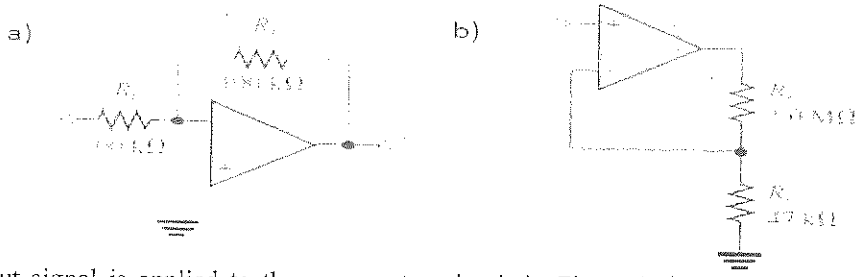
(a) JFET biased (b) Family of drain characteristic curves

e) For the JFET in Figure below, $V_{GS(off)} = -4$ V and $I_{DSS} = 12$ mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation when $V_{GS} = 0$ V. **(4 marks)**



Question 5: Operational Amplifiers / Op-amp circuits [15 marks]

a) If a signal voltage of 10 mV rms is applied to each amplifier in Figure below, what are the output voltages and what is their phase relationship with inputs? **(10 marks)**



b) The input signal is applied to the comparator circuit in Figure below. Draw the output showing its proper relationship to the input signal. Assume the maximum output levels of the comparator is ±14V. **(5 marks)**

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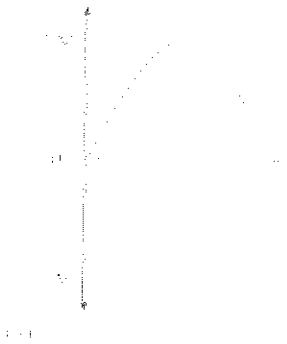

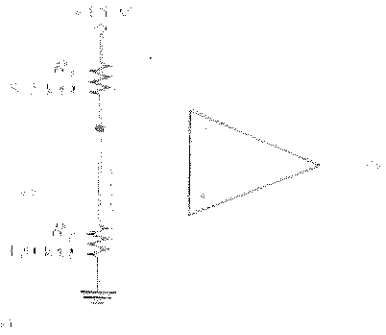

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Formulas

$r = \frac{V_{r(pp)}}{V_{DC}}$ Ripple factor

$V_{r(pp)} \cong \left(\frac{1}{fR_LC}\right)V_{pi(max)}$ Peak-to-peak ripple voltage, capacitor-input filter

$V_{DC} = \left(1 - \frac{1}{2fR_LC}\right)V_{pi(max)}$ DC output voltage, capacitor-input filter

$I_E = I_C + I_B$ Transistor cur

$\beta_{DC} = \frac{I_C}{I_B}$ DC current ga

$r'_e \cong \frac{25\text{ mV}}{I_E}$ Internal ac emitter resistance

Common-Emitter

$R_{in(base)} = R_1 \| R_2 \| R_{in(base)}$ Total amplifier input resistance, voltage-divider bias

$R_{in(base)} = \beta_{ac} r'_e$ Input resistance at base

$A_v = \frac{R_c}{r'_e}$ Voltage gain, base-to-collector, unloaded

$A_v = \frac{R_c}{r'_e + R_E}$ Voltage gain without bypass capacitor

$A_v = \frac{R_c}{r'_e}$ Voltage gain, base-to-collector, loaded, bypassed R_E

$\text{Attenuation} = \frac{V_b}{V_o} = \frac{R_c + R_{in(base)}}{R_{in(base)}}$

overall voltage gain of the amplifier, $A_v = \left(\frac{V_c}{V_b}\right)\left(\frac{V_b}{V_s}\right) = \frac{V_c}{V_s}$

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