FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE & TECHNOLOGY (CEST)

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

CERTIFICATE IV IN ELECTRONIC ENGINEERING

EEE412- DIGITAL ELECTRONICS 1

FINAL EXAMINATION – TRIMESTER 2, 2016

DATE: As per timetable **TIME:** As per timetable

TIME ALLOWED: 2 HOURS

INSTRUCTIONS TO STUDENTS

1. *You are allowed 10 minutes Extra reading time during which you are NOT to write.*
2. *Begin each section on a new page and use both sides of the sheet.*
3. *Write your candidate-number at the top of each attached sheet.*
4. *Insert all written foolscaps, graph paper, drawing paper, etc. in their correct sequence and secure with string.*
5. *For all sheets of paper on which rough/draft work has been done, cross each one through and ATTACH these to your answer scripts.*
6. *Write clearly the number(s) of the question(s) attempted on the top of each sheet.*
7. *ANSWER ALL QUESTIONS.*
8. *Show all working clearly where necessary.*
9. *Programmable calculators are not allowed, especially the ones that does the conversions of number systems.*
10. ALWAYS CHECK YOUR WORK BEFORE YOU LEAVE THE ROOM!

Section A – Multiple Choice [20 marks]

Choose the appropriate answer from each question by writing the alphabet beside the question number in your answer booklet.

1. The simplification of the Boolean expression $\overline{\overline{A}B\overline{C}} + \overline{A\overline{B}C}$ is;
   A. 0
   B. 1
   C. A
   D. BC

2. What is the total number of possible combinations of binary inputs to a gate having three input variables?
   A. 2
   B. 4
   C. 8
   D. 16

3. How many Flip-Flops are required for mod–16 counter?
   A. 5
   B. 6
   C. 3
   D. 4

4. The digital logic family which has minimum power dissipation is;
   A. TTL
   B. RTL
   C. DTL
   D. CMOS

5. The SOP form of the Boolean expression A + B(D + CE) + F is;
   A. (A + B)(BCD + BEF)
   B. AB + BCD + BE + BF
   C. (A + B)(B + C + D)(B + E + F)
   D. A + BD + BCE + F

Please turn over

6. The Boolean expression $A+\overline{B}+C$ is a;
    A. Sum term
    B. Literal term
    C. Product term
    D. Complemented term

7. The hexadecimal equivalent for the binary number 110111110101001 is;
    A. 6FA9
    B. 28585
    C. DF51
    D. DF52

8. When simplified with Boolean Algebra (X + Y)(X + Z) simplifies to;
    A. X
    B. X + X(Y + Z)
    C. X(1 + YZ)
    D. X + YZ

9. A device which converts BCD to Seven Segment is called;
    A. Encoder
    B. Decoder
    C. Multiplexer
    D. De-multiplexer

10. The binary number 1011 is equal to the decimal number

    A. 13
    B. 49
    C. 11
    D. 3

11. What is the weight of digit 6 in the decimal number 1386?
    A. 1
    B. 2
    C. 3
    D. 0

12. The Boolean expression for a 4-input NOR gate is;
    A. A + B + C + D
    B. ABCD
    C. $\overline{A+B+C+D}$
    D. $\overline{ABCD}$

Please turn over

13. Determine the value of **B** that make the product term $A\overline{B}C\overline{D}$ equal to 1.
    A. B = 0
    B. B = 1
    C. B = 1010
    D. B = 0101

14. The output of a logic gate is 1 when all its inputs are at logic 0. The gate is either;
    A. a NAND or an EX-OR
    B. an OR or an EX-NOR
    C. an AND or an EX-OR
    D. a NOR or an EX-NOR

15. When are the outputs, INVALID for an S-R Flip-Flop?
    A. S = 0, R = 0
    B. S = 1, R = 1
    C. S = 1, R = 0
    D. S = 0, R = 1

16. Applying DeMorgan's theorem to the expression $\overline{A+B+C}$ will give;
    A. $\overline{ABC}$
    B. $\overline{A}+\overline{B}+\overline{C}$
    C. $\overline{A}\overline{B}\overline{C}$
    D. $A+B+C$

17. Universal Gates can be used to perform an INVERTER operation by;
    A. ANDing two 2-input NOR gates
    B. Shorting the inputs of a 2-input NAND gate
    C. Using a 2-input NOR gate as a NAND gate
    D. Using a 2-input NAND gate as a NOR gate

18. How many gates would be required to implement the Boolean expression XY + X(X+Z) +Y(X+Z) before simplification?
    A. 3
    B. 5
    C. 6
    D. 8

Please turn over

19. A group of flip-flops used for data storage is called;
    A. Registers
    B. JK Flip-flop
    C. Latch
    D. Counter

20. Which of the following Boolean expressions describes Distributive Law;
    A. AB = BA
    B. A = A + A
    C. A + (B + C) = (A + B) + C
    D. A + B(C + D) = A + BC + BD

Section B – True or False (10 marks)

1. In a positive logic system, logic state 1 corresponds to higher voltage level.

2. Karnaugh map is used for the purpose to maximize the terms of a given a Boolean expression.

3. 2 two-input AND gates and 2 two-input OR gates are required to realize the Boolean expression Y = CD + EF + G.

4. Logic Probe is used to determine the logic state of an output of a logic gate.

5. The minimum SOP expression derived from the Karnaugh map below is $\overline{W}\,\overline{X} + WY$.

YZ \ WX	00	01	11	10
00	1			
01	1		1	1
11	1		1	1
10	1			

6. A NOR gate output is LOW when all inputs are HIGH.

7. The count for a MOD 10 counter is from 0 to 9.

Please turn over

8. A negative edge triggered J-K flip-flop will TOGGLE on the rising edge of the clock pulse when both the inputs J and K are tied HIGH.

9. The largest decimal number that can be represented in binary with six bits is 64.

10. Propagation Delay Time is the interval of time required after an input signal has been applied for the resulting output change to occur.

Section C – Short Answers [20 marks]

1. Draw the switch equivalent circuits for the equivalent logic function of an;
   A. AND Gate (2 marks)
   B. OR Gate (2 marks)

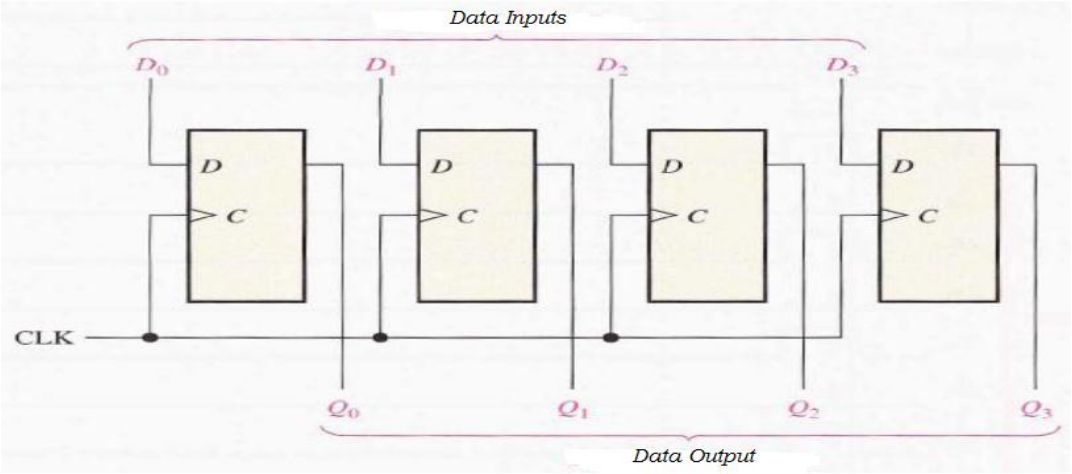
2. Convert the Boolean expression, $\overline{\overline{(A+B)}+C}$ to SOP form. (2 marks)

3. Convert the binary number 11000110 to Gray code. (2 marks)

4. Explain the following threshold voltage acronyms;
   A. V_{IL}
   B. V_{OH} (2 marks)

5. What is the difference between a CMOS and a TTL integrated circuit (IC) in terms of their operating voltages? (1 mark)

6. Identify the following circuit shown below;



Please turn over (1 mark)

7. Develop a truth table for the POS expression; $(\overline{A}+\overline{B}+\overline{C})(A+B+C)(A+\overline{B}+C)$. (2 marks)
8. Use the Karnaugh map to find the minimum SOP form for the expression; $\overline{A}\overline{B}\overline{C}+A\overline{B}\overline{C}+\overline{A}B\overline{C}+AB\overline{C}$. (2 marks)
9. Express the decimal number 106.58 as a sum of products obtained by multiplying each digit by its appropriate weight. (2 marks)
10. Give atleast two advantages of Digital over Analog representation. (2 marks)

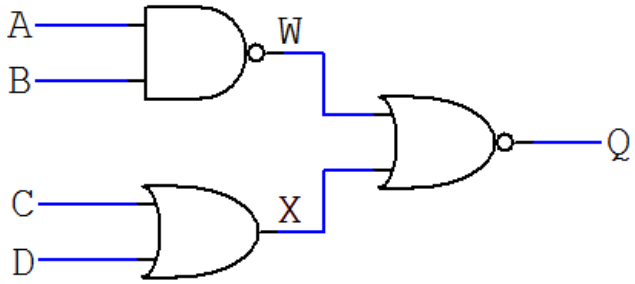
Section D – Calculations & Diagrams (40 marks)

Show your working clearly where necessary.

1. Convert the decimal number 127 to the following numbers using any of the conversion methods.
   A. Binary number (2 marks)
   B. Hexadecimal number (1 mark)
   C. Octal number (1 mark)

2. Implement each expression given below as originally stated with appropriate logic gates. Then implement the simplified expression, and compare the number of gates.
   A. $(A+\overline{B})(A+C)$ (4 marks)
   B. $AB+A(B+C)+B(B+C)$ (4 marks)

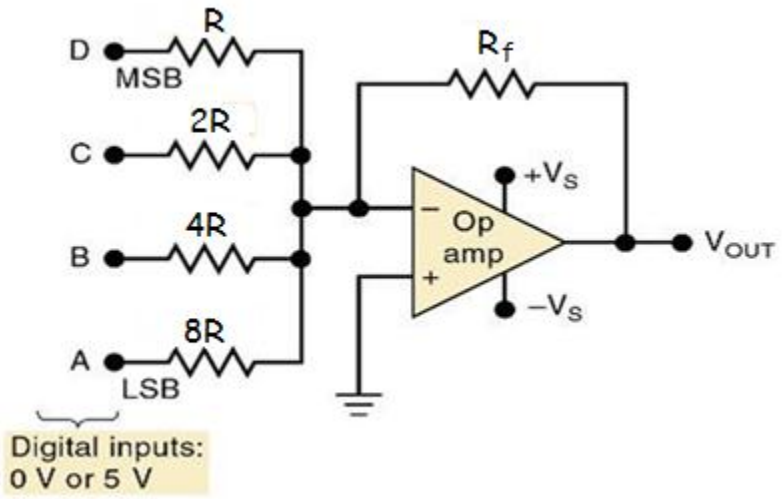
3. For the Logic Gates Circuit shown below;



   A. Write down the Logic Expression for W, X and Q. (3 marks)
   B. Determine the Truth Table for the circuit. (4 marks)

Please turn over

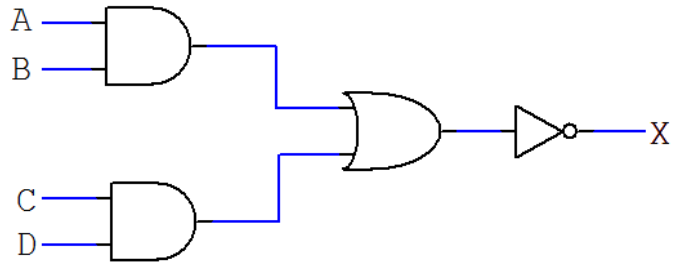
4. A weighted-resistor DAC has R_F= 10KΩ and R=2KΩ.



Calculate its output voltage when the 4-bit digital input is **1010**. *Note: Logic 1 voltage = 5 volts.* (2 marks)

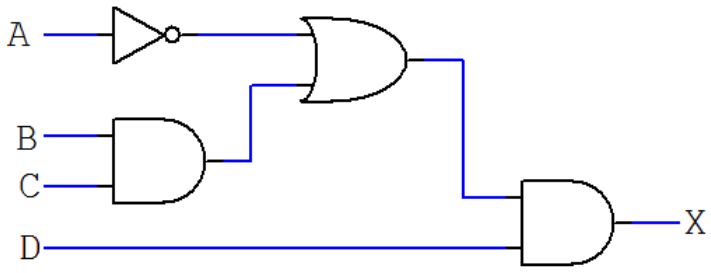
5. Write the Boolean expression for each of the logic circuits shown below;

A.



(2 marks)

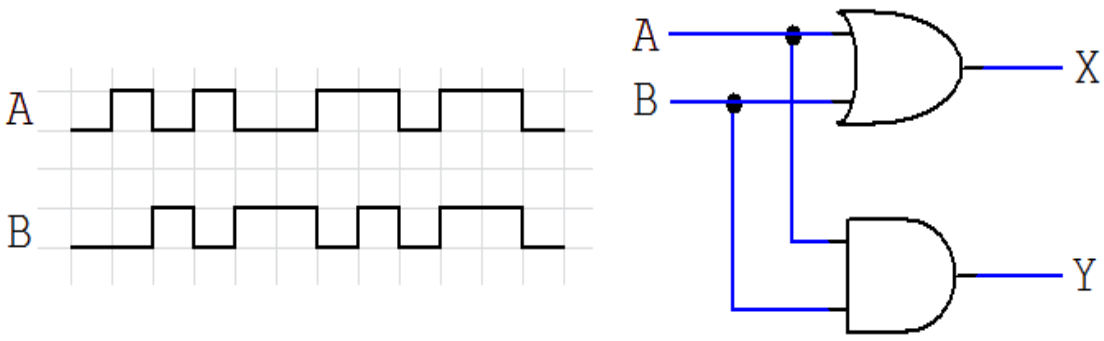
B.



(2 marks)

Please turn over

6. Determine the output waveforms for the AND gate and for the NOR gate, given the input waveforms A and B as below. (4 marks)



7. Construct a mod-12 negative edge triggered ripple counter using JK Flip-flops.
   Draw;
   A. The circuit diagram of the mod-12 counter. (3 marks)
   B. The timing diagram for one cycle of the count. (4 marks)

8. Apply DeMorgan's theorem to each expression;
   A. $\overline{(A+B+C)D}$ (2 marks)
   B. $\overline{\overline{(A+B)}+\overline{C}}$ (2 marks)

Section E – Application Questions (10 marks)

1. Three switches A, B, C control a device. The device must operate if A is on and B is on but C is off, or if A is off B is on and C is on, or if A is on B is off and C is on. Under all other conditions the device must NOT operate. Take Q as the output.
   A. Draw the truth table (3 marks)
   B. Write the Boolean expression (2 marks)

2. A manufacturing plant uses two tanks to store a certain liquid chemical that is required in a manufacturing process. Each tank has a sensor that detects when the chemical level drops to 25% full. The sensors produce a 5V level when the tanks are more than one-quarter full. When the volume of chemical in a tank drops to one-quarter full, the sensor puts out a 0V level.

It is required that a single green light-emitting diode (LED) on an indicator panel show when both tanks are more than one-quarter full. Show with an aid of a diagram, and briefly explain how a NAND gate can be used to implement this function. (5 marks)

The End

----------GOOD LUCK----------