FNU FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE AND TECHNOLOGY

School of Electrical & Electronics Engineering

Trade Diploma in Electronics Engineering

EEE551 – Digital Electronics II

FINAL EXAMINATION

Trimester 1, 2016

Date: As per Exam Time Table

Time: As per Exam Time Table (3 hours)

Venue: As per Exam Timetable

Instructions to Students

1. You are allowed an extra ten (10) minutes of reading time during which you are NOT allowed to write.
2. Attempt ALL questions in this examination booklet
3. Write your answers in the answer booklet provided.
4. Write your Student ID number on each page used.
5. Begin each Section on a fresh page and use both sides of the answer sheet.
6. You may use calculators provided they are non-programmable.
7. Clearly number the questions in your answer paper in their correct sequence and write legibly. Show all working.
8. Attach any extra sheets used to your answer booklet securely with the string provided.

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Question 1: (Logic families) [10 marks]

A) From the table given below, determine the noise margins when a 74ALS device is driving a 74AS input. [3 marks]

Typical TTL series characteristics.

	74	74S	74LS	74AS	74ALS	74F
Performance ratings						
Propagation delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Max. clock rate (MHz)	35	125	45	200	70	100
Fan-out (same series)	10	20	20	40	20	33
Voltage parameters						
V_{OH}(min) (V)	2.4	2.7	2.7	2.5	2.5	2.5
V_{OL}(max) (V)	0.4	0.5	0.5	0.5	0.5	0.5
V_{IH}(min) (V)	2.0	2.0	2.0	2.0	2.0	2.0
V_{IL}(max) (V)	0.8	0.8	0.8	0.8	0.8	0.8

B) Define: [1 mark]
i) Noise Margin & Noise Immunity
ii) Propagation delay

C) Describe the difference between current sinking and current sourcing. [1 mark]

D) Compare the electrical characteristic of TTL and CMOS. [2 marks]

E) Name 3 important parameters for evaluating and comparing logic families. [2 marks]

F) What can happen if a TTL output is connected to more gate inputs than it is rated to handle. [1 mark]

Question 2: (Multiplexers/Decoders) [15 marks]

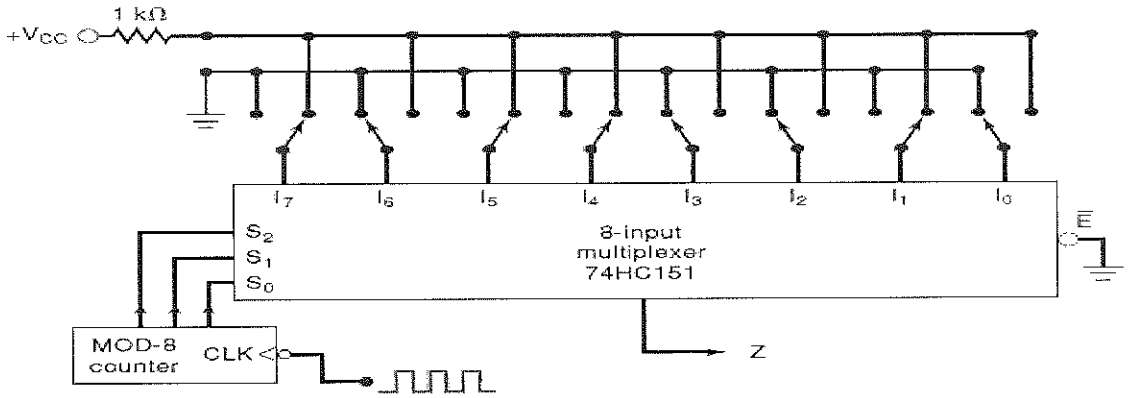
A) Consider a 3-input and 2 output system depicted as follows: [3 marks]
Implement the system using 74154 decoder.

x3	x2	x1	y1	y2
0	0	0	1	d
0	0	1	d	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	1
1	0	1	1	1
1	1	0	0	1
1	1	1	d	0

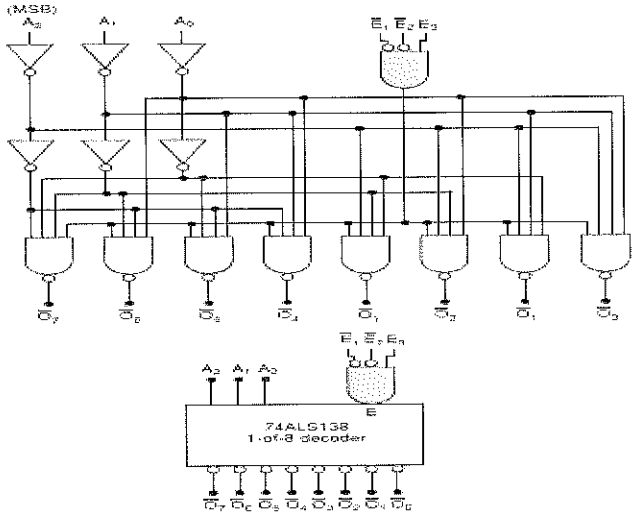
Please Turn Over

B) Consider the 3-input(X_3 X_2 X_1) system given by :
$y = \Sigma(0,1,2,4,7)$
Draw a 74LS151, 8-input multiplexer based circuit that realizes the system. [3 marks]

C) Figure below shows how a multiplexer can be used to generate logic waveforms with any desirable pattern. The pattern is programmed using eight SPDT switches, and the waveform is repetitively produced by pulsing the MOD-8 counter.
i) Draw the waveform at *Z* for the given switch positions with respect to the clock cycle.
ii) Draw the truth table for output Z
[4.5 marks]



D) Refer to the Figure below and determine the levels at each decoder output for the following sets of input conditions. [2 marks]
i) All inputs high except E3= low.
ii) All inputs low except E1'=E2'=high.



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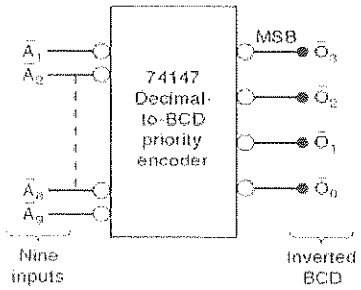
E) Refer to the priority encoder below and determine the output levels for the 74147 encoder when A6' = A7'=0 and all other inputs are high. [2.5 marks]



74147 decimal-to-BCD priority encoder.

$\bar{A}_1$	$\bar{A}_2$	$\bar{A}_3$	$\bar{A}_4$	$\bar{A}_5$	$\bar{A}_6$	$\bar{A}_7$	$\bar{A}_8$	$\bar{A}_9$	$\bar{O}_3$	$\bar{O}_2$	$\bar{O}_1$	$\bar{O}_0$
1	1	1	1	1	1	1	1	1	1	1	1	1
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	0	1	0	1	1	1
X	X	X	X	X	X	0	1	1	1	0	0	0
X	X	X	X	X	0	1	1	1	1	0	0	1
X	X	X	X	0	1	1	1	1	1	0	1	0
X	X	X	0	1	1	1	1	1	1	0	1	1
X	X	0	1	1	1	1	1	1	1	1	0	0
X	0	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0

X = either 0 or 1

Question 3: (Combinational logic circuits) [15 marks]

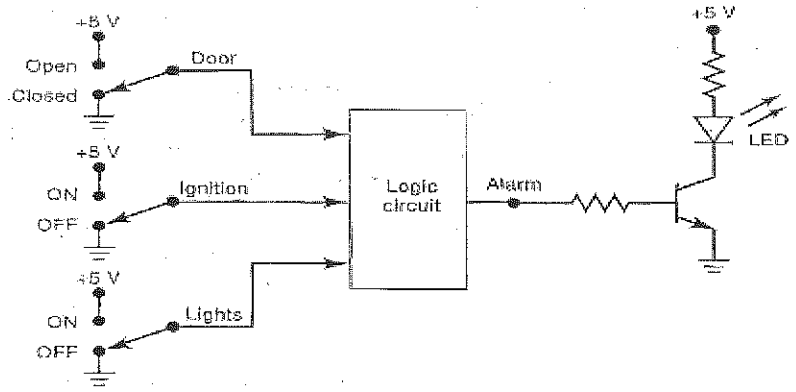
A) A 4-input, single output combinational system is given by: [5 marks]

Y = f(X4, X3, X2, Xl) = X4' X3 X1 + X3 X2 X1' + X4' X2 + X4 X1

i) Draw the Karnaugh map representation for this system.
ii) Draw the Truth Table representation for the system.

B) Figure below shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver seat, the ignition, and the headlights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:

- The headlights are on while the ignition is off.
- The door is open while the ignition is on. [5 marks]



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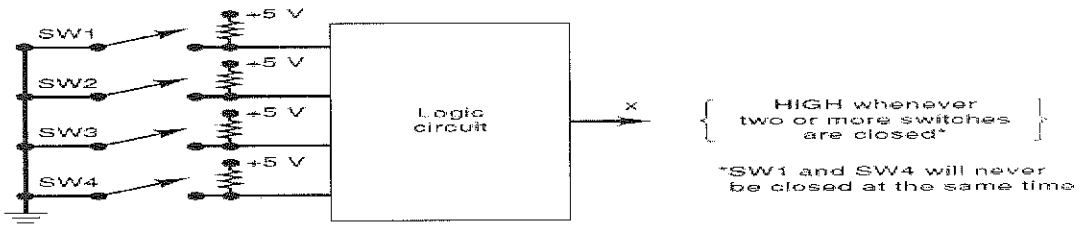
C) Figure below shows four switches that are part of the control circuitry in a copy machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open, and as the paper passes over a switch, the switch closes. It is impossible for switches SW1 and SW4 to be closed at the same time. Design the logic equation to produce a HIGH output whenever two or more switches are closed at the same time. [5 marks]



Question 4: (Sequential logic circuit / Counters) [27.5 marks]

A) What flip-flop (FF) outputs should be connected to the clearing NAND gate to form a MOD-13 counter. [2.5 marks]

B) Draw a 3 bit synchronous, up/down counter. The count direction is controlled by switch dir (dir = 1 to count up and dir = 0 to count down). Once count 8 is reached the counter should reset to zero on next clock pulse if dir=1 or decrement by 1 if dir=0 and while on count zero if dir =0, the counter should remain at zero. Use D flip-flop based system and implement the system. (Show state diagram, K-map and circuit implementation). [15 marks]

C) A four-bit ripple counter is driven by a 20 MHz clock signal. Each FF has $t_{pd} = 20$ ns.
   i) What is the maximum clock frequency that can be used with this counter.
   ii) What would f_{max} be if the counter were expanded to six bits.
   [3.5 marks]

D) A 8-bit ripple counter has a 256-kHz clock signal applied. [5 marks]
   (i) What is the MOD number of this counter.
   (ii) What will be the frequency at the MSB output.

E) Assume that a five-bit binary counter starts in the 00000 state. What will be the count after 144 input pulses. [1.5 marks]

Question 5: (Arithmetic circuits) [12.5 marks]

A) i) Write a function table for a half adder (inputs A and B; outputs SUM and CARRY). From the function table design a logic circuit that will act as a half adder.
ii) A full adder can be implemented in many different ways. Implement full adder using half adders. (Note: can use half adder block diagrams)
[6 marks]

Please Turn Over

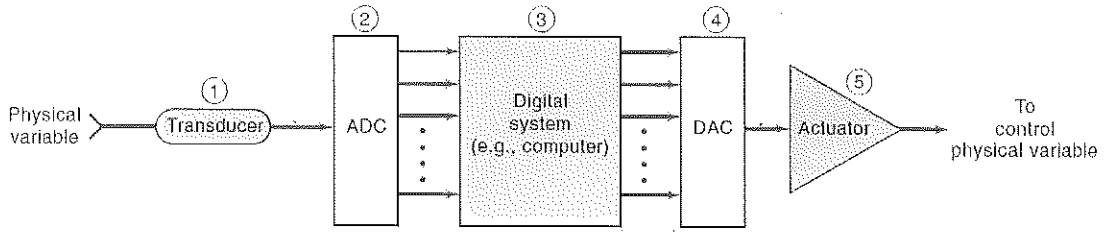
B) What is the range of signed decimal values that can be represented in a byte. [2 marks]
C) How many bits are required to represent decimal values ranging from -40 to 40. [2.5 marks]
D) Add the hex numbers 89F + 2A4. [2 marks]

Question 6: (Memory devices/display devices) [10 marks]

A) A certain memory has a capacity of 2K * 8. [3 marks]
   i) What is the number of bits per word.
   ii) How many words does it store.
   iii) How many memory cells does it contain.
B) Compare main memory of computer with auxiliary memory. [2 marks]
C) Define Byte. [1 marks]
D) Indicate which of the following refers to LCD display and which refers to LED display.
   i) Emit light
   ii) Reflect ambient light
   iii) Are best for low-power application
   iv) Require an ac voltage
   v) Use a 7-segment arrangement to produce digits
   vi) Require current-limiting resistors [4 marks]

Question 7: (DAC/ADC and PLD) [10 marks]

A) Explain Quantization error. [1 mark]
B) What is the largest value of output voltage from an eight-bit DAC that produces 2.0V for a digital input 00110010. [1 mark]
C) Outline the function of each block in the Figure below. [2 marks]



D) A five-bit D/A converter produces V_{OUT} = 0.4 V for a digital input of 00001. What is the resolution (step size) of the DAC. Describe the staircase signal out of this DAC. [2 marks]
E) The Figure below shows the general type of ADC. What is the function of Register and D/A converter in the ADC. [2 marks]

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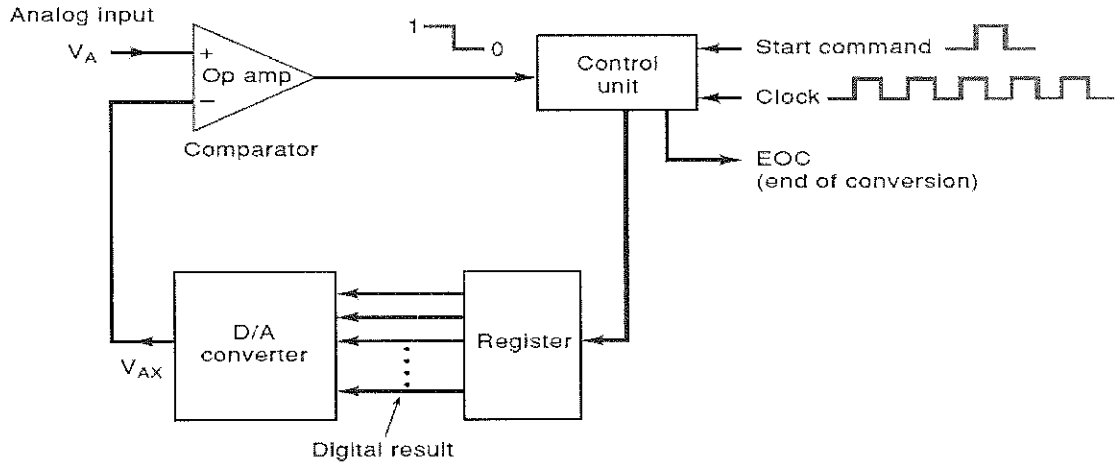

F) What are the three major categories of digital system and describe each. [2 marks]

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Appendix

Excitation Table for FFs

q	Q	S	R	J	K	D	T
0	0	0	d	0	d	0	0
0	1	1	0	1	d	1	1
1	0	0	1	d	1	0	1
1	1	d	0	d	0	1	0

Formulas

$T_{clock} \geq N \times t_{pd}$ For proper operation of ripple counter

$f_{max} = \frac{1}{N \times t_{pd}}$ Maximum frequency of ripple counter

SN54154, SN74154
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

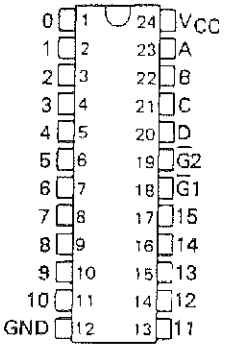
SDLS056

DECEMBER 1972 – REVISED MARCH 88

- '154 is Ideal for High-Performance Memory Decoding
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input Line to Any One of 16 Outputs
- Input Clamping Diodes Simplify System Design
- High Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL and MSI Circuits

TYPICAL AVERAGE PROPAGATION DELAY		TYPICAL POWER DISSIPATION
3 LEVELS OF LOGIC	STROBE	
23 ns	19 ns	170 mW

SN54154 . . . J OR W PACKAGE
SN74154 . . . N PACKAGE
(TOP VIEW)



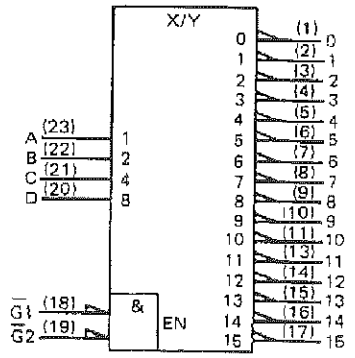
description

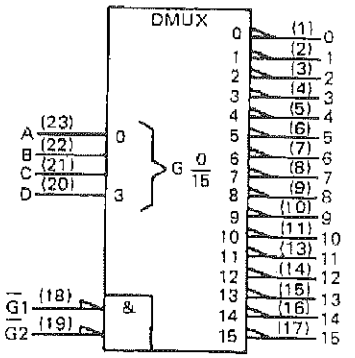
Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, $\overline{G1}$ and $\overline{G2}$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. For ultra-high speed systems, SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

These circuits are fully compatible for use with most other TTL circuits. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

The SN54154 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74154 is characterized for operation from 0°C to 70°C.

logic symbols (alternatives)†





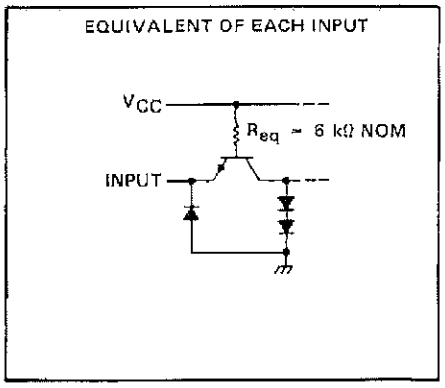
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

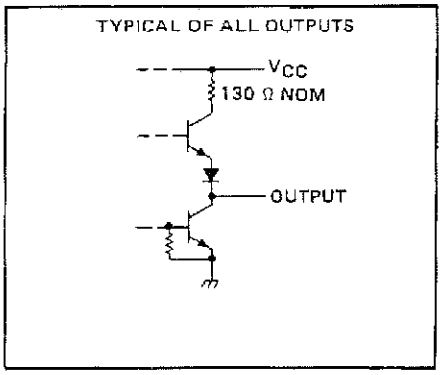
FUNCTION TABLE

INPUTS						OUTPUTS														
$\overline{G}1$	$\overline{G}2$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

schematics of inputs and outputs





8-input multiplexer

74ALS151

FEATURES

- 8-to-1 multiplexing
- On chip decoding
- Multi-function capability
- Complementary outputs
- See 74ALS251 for 3-State version

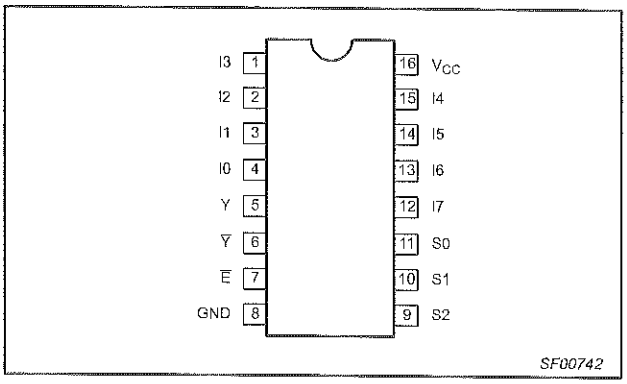
DESCRIPTION

The 74ALS151 is a logic implementation of a single 8-position switch with the switch position controlled by the state of three select (S0, S1, S2) inputs. True (Y) and complementary ($\overline{Y}$) outputs are both provided.

The enable ($\overline{E}$) is active-Low. When $\overline{E}$ is High, Y output is Low and the $\overline{Y}$ output is High regardless of all other inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS151	8.0ns	8.0mA

PIN CONFIGURATION



ORDERING INFORMATION

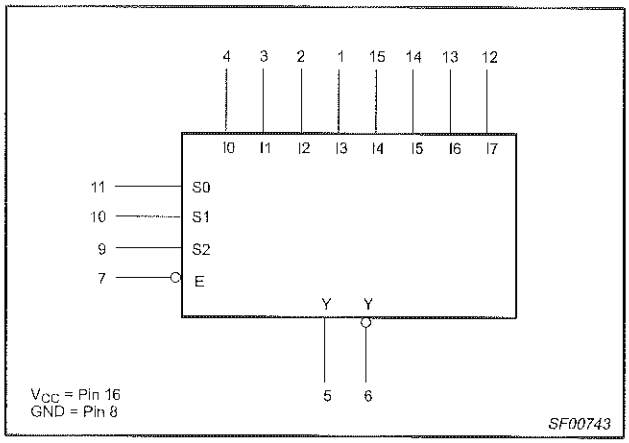
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74ALS151N	SOT38-4
16-pin plastic SO	74ALS151D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

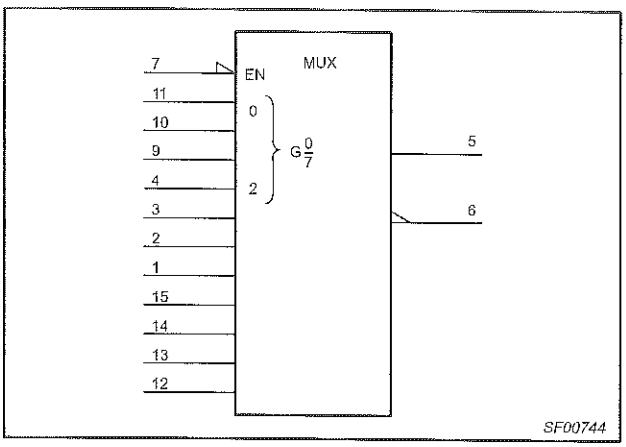
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0 – I7	Data inputs	1.0/1.0	20µA/0.1mA
S0 – S2	Select inputs	1.0/1.0	20µA/0.1mA
$\overline{E}$	Enable input (active-Low)	1.0/1.0	20µA/0.1mA
Y, $\overline{Y}$	Data outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

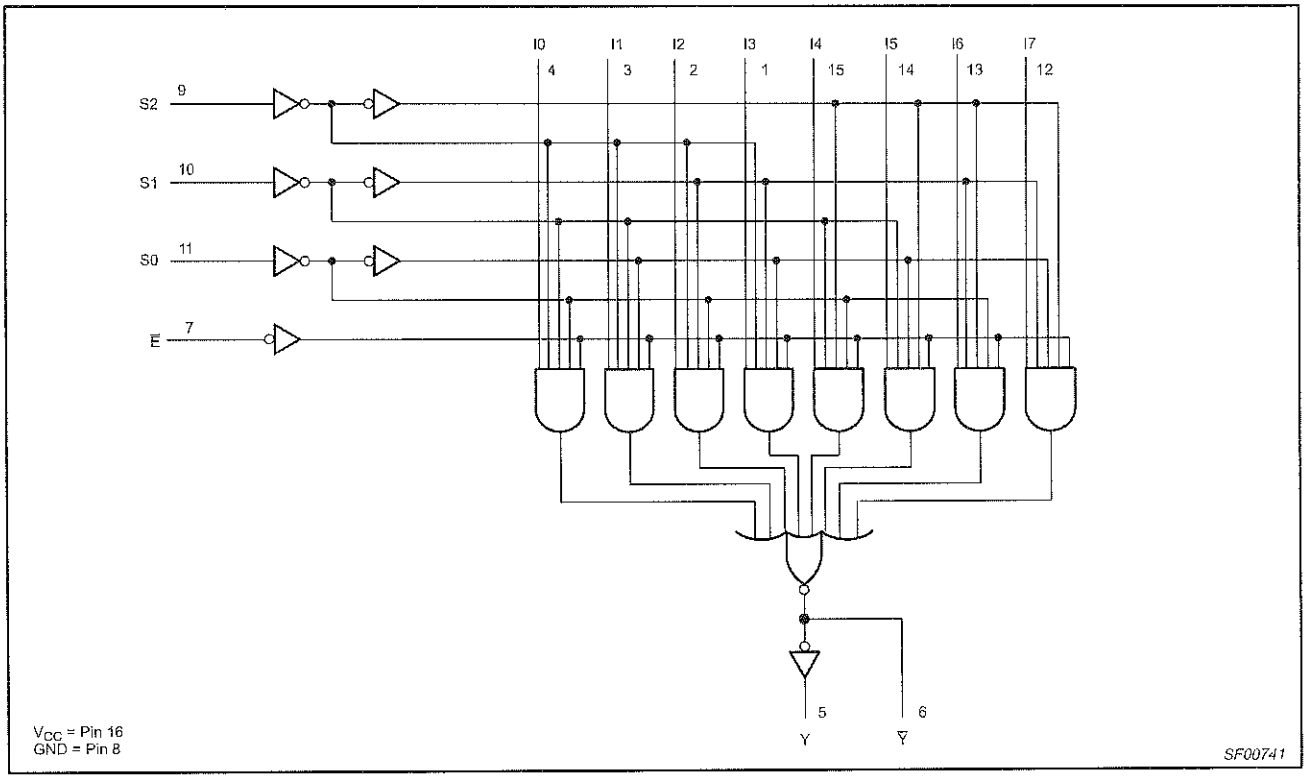
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
S2	S1	S0	$\overline{E}$	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I0	$\overline{I0}$
L	L	H	L	I1	$\overline{I1}$
L	H	L	L	I2	$\overline{I2}$
L	H	H	L	I3	$\overline{I3}$
H	L	L	L	I4	$\overline{I4}$
H	L	H	L	I5	$\overline{I5}$
H	H	L	L	I6	$\overline{I6}$
H	H	H	L	I7	$\overline{I7}$

H = High voltage level
L = Low voltage level
X = Don't care