FNU FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

TRADE DIPLOMA IN ELECTRICAL ENGINEERING

EEE543 – DIGITAL AND ANALOG ELECTRONIC ENGINEERING.

FINAL EXAMINATION – TRIMESTER 1 - 2016.

TIME: TBA **Date: TBA** **No. of Pages = 7**

INSTRUCTIONS TO STUDENTS:

1. You are allowed 10 minutes **EXTRA** as reading time during which you are **NOT** to write.
2. Begin each answer on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each attached sheet.
4. Insert all written foolscap, graph paper, drawing paper, etc. in their correct sequence and secure well.
5. For all sheets of paper on which rough/draft work has been done, cross it through and attach to your answer scripts.
6. Show all workings where necessary
7. Diagrams and graphs can be drawn in pencil.
8. Non- programmable calculators are allowed.
9. Attempt all questions, i.e. Sections A, B and C
10. **Check your work before you leave the room!!**

Section A: **(20 marks)**

Part 1 MULTIPLE CHOICE **(10 marks)**

Attempt all questions in this section by selecting and writing the correct alphabet beside the number.

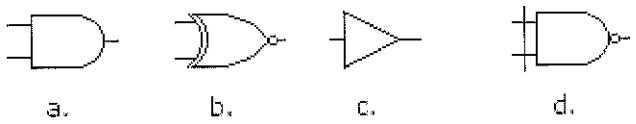
1. Convert BCD 0001 0010 0110 to binary?

   (a) 1111110
   (b) 1111101
   (c) 1111000
   (d) 1111111

2. In a JK synchronous Flip Flop, if J = 1 and K = 1 then Q will

   (a) Change to 0 if it was on 1
   (b) Toggle
   (c) Remain on 1
   (d) not allowed

3. Which of the figures shown below represents the exclusive-NOR gate?



   (a) A (b) B (c) C (d) D

4. Which among the below stated Boolean expressions do not obey De-Morgan's theorem

   a. $\overline{X+Y} = \overline{X} \cdot \overline{Y}$
   b. $\overline{X.Y} = \overline{X} + \overline{Y}$
   c. $X.Y = \overline{X+Y}$
   d. None of the above

5. Output will be LOW for any case when one or more inputs are zero for a(n);
   (a) OR gate
   (b) NOT gate
   (c) AND gate
   (d) NOR gate

6. Which of the following statements accurately represents the best two methods of logic simplication?

(a) Boolean algebra and Karnaugh mapping
(b) Karnaugh mapping circuit waveform analysis
(c) Actual circuit trial and error evaluation and waveform analysis
(d) Boolean algebra and actual circuit trial and error evaluation

7. Which statement below best describes a Karnaugh map?

(a) A Karnaugh map can be used to remove Boolean rules.
(b) The Karnaugh map eliminates the need for using NAND and NOR gates.
(c) Variable compliments can be eliminated by using Karnaugh maps.
(d) Karnaugh maps provide a visual approach to simplifying Boolean expressions.

8. Which of the following expressions is in the product-of-sums form?

(a) (A+B)(C+D)
(b) (AB)(CD)
(c) AB(CD)
(d) AB + CD

9. The output of an AND gate with three inputs A, B and C, is HIGH when;

(a) A=1, B=1, C=0
(b) A=0, B=0, C=0
(c) A=1,B=1,C=1
(d) A=1,B=0,C=1

10. Which of the following gates are added to the input of the OR gate to convert it to the NAND gate

(a) NOT
(b) AND
(c) OR
(d) XOR

Part 2 **NUMBER CONVERSIONS** **(10 marks)**

Convert the following;

a) Decimal 4926 to BCD code (2 marks)
b) BCD 100001110001 to Decimal (2 marks)
c) Binary 11101 Gray code (2 marks)
d) Gray 1010 to Binary (2 marks)
e) Decimal 593 to Excess-3 code (2 marks)

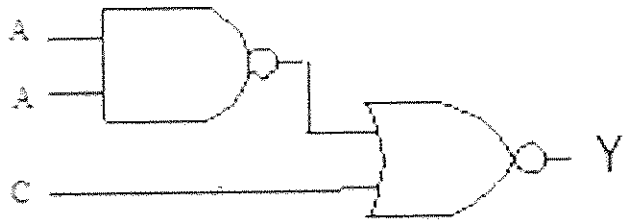
Section B

Combinational Circuits & Logic Families (TTL & CMOS) (20 marks)

Question 1

a) Draw the combinational logic circuit for the Boolean expression $Q = \overline{(AB)}.\overline{(A+B)}.C$ **(3 marks)**

b) From the combination logic circuit below find the simplified Boolean expression. **(3 marks)**



c) From the given truth table find the simplified Boolean expression and draw the combinational logic circuit. **(5 marks)**

C	B	A	O P
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Question 2

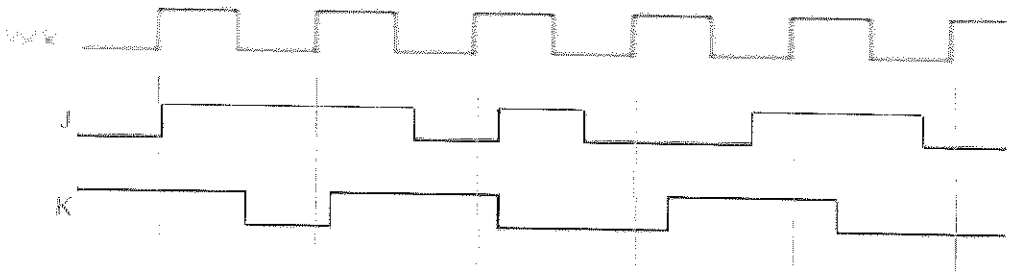
a) Describe the full operation of the TTL circuit operation when output is in "LOW STATE" **(8 Marks)**
b) What is the input range of the TTL circuit when the inputs are low? **(1 mark)**

Section C Flip Flops & Display Devices (20 marks)

Question 1

a) Draw and explain the full operation of the SR NAND gate flip flop **(5 marks)**

b) Draw Q and Q' in the JK flip flop timing diagram below; **(5 marks)**



Question 2

A customer wishes to purchase a SSD display which has a luminous intensity of 1.5. Use the common anode circuit to test its brightness using digit "4". **(10 marks)**

SECTION D

Rectifiers and Karnaugh Map **(20 marks)**

Question 1

a) Explain the full operation of the centre-tapped full-wave rectifier with input waveform and also the rectified output waveform.
(7 marks)

b) Assume that the total voltage across the high-voltage secondary of a transformer used to supply a full-wave rectifier is 300 volts. Find the average load voltage (ignore the drop across the diode). (2 marks)

c) Write one difference between the centre-tapped and bridge rectifiers (1 marks)

Question 2

a) Find the simplified Boolean expression from the Karnaugh map below;
(5 marks)

	C'D'	C'D	CD	CD'
A'B'			1	1
A'B				
AB				
AB'	1			1

b) Find the simplified Boolean expression from the Karnaugh map below;
(5 marks)

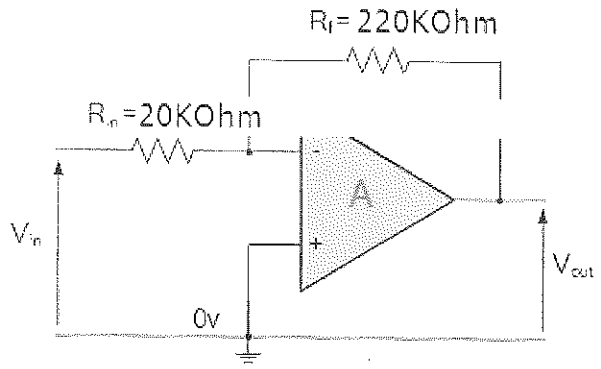
	C'D'	C'D	CD	CD'
A'B'				
A'B	1	1	1	1
AB	1	1	1	1
AB'				

Section E Op – Amps & Power Supplies (20 marks)

Question 1

a) Describe the operation of the Differential Amplifier (6 marks)

b) A Non- Inverting Op-amp circuit is given below;



Calculate the closed loop gain of the circuit? (5 marks)

Question 2

a) Draw a labeled Power Supply diagram using a Zener diode (5 marks)
b) What is the function of this Zener diode in the power supply? (2 marks)
c) What is the function of the capacitor in the power supply? (2 marks)

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