FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE AND TECHNOLOGY

School of Electrical & Electronics Engineering

Bachelor of Engineering (Electrical & Electronics)

EEE627 – Logic Design

FINAL EXAMINATION

Semester 1, 2016

Date: As per Exam Time Table

Time: As per Exam Time Table (3 hours)

Venue: As per Exam Timetable

Instructions to Students

1. You are allowed an extra ten (10) minutes of reading time during which you are NOT allowed to write.
2. Attempt ALL questions in this examination booklet
3. Write your answers in the answer booklet provided.
4. Write your Student ID number on each page used.
5. Begin each Section on a fresh page and use both sides of the answer sheet.
6. You may use calculators provided they are non-programmable.
7. Clearly number the questions in your answer paper in their correct sequence and write legibly. Show all working.
8. Attach any extra sheets used to your answer booklet securely with the string provided.

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Final Examination

Section A: Multiple Choices [12 marks]
Choose the letter of the BEST choice.

1. If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output?

   a) 1
   b) 2
   c) 7
   d) 8

2. Output will be a LOW for any case when one or more inputs are zero for a:

   a) OR gate
   b) NOT gate
   c) NOR gate
   d) AND gate

3. Which of the following statements does NOT describe an advantage of digital technology?

   a) The values may vary over a continuous range.
   b) The circuits are less affected by noise.
   c) The operation can be programmed.
   d) Information storage is easy.

4. Give the decimal value of binary 10010.

   a) 6_{10}
   b) 9_{10}
   c) 18_{10}
   d) 20_{10}

5. How is a J-K flip-flop made to toggle?

   a) J = 1, K = 1
   b) J = 1, K = 0
   c) J = 0, K =1
   d) J = 0, K = 0

6. SPLDs, CPLDs, and FPGAs are all which type of device?

   a) PAL
   b) PLD
   c) EPROM
   d) SRAM

Please Turn Over

7. The difference between a PLA and a PAL is:

   a) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane.
   b) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane.
   c) The PAL has more possible product terms than the PLA.
   d) PALs and PLAs are the same thing.

8. Convert binary 111111110010 to hexadecimal.

   a) $EE2_{16}$
   b) $FF2_{16}$
   c) $2FE_{16}$
   d) $FD2_{16}$

9. Why have PLDs taken over so much of the market?

   a) One PLD does the work of many ICs.
   b) The PLDs are cheaper.
   c) Less power is required.
   d) All of the above

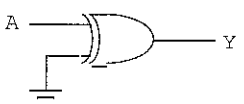
10. How many times can a GAL be erased and reprogrammed?

    a) 0
    b) At least 100
    c) At least 1000
    d) Over 10,000

11. FPGA is the acronym for _____.

    a) Flexible Programming [of] Generic Assemblies
    b) Field Programmable Generic Array
    c) Field Programmable Gate Array
    d) Field Programmer's Gate Assembly

12. The output of this circuit is always _____.



    a) 1
    b) 0
    c) A
    d) $\overline{A}$

Please Turn Over

Section B: Short Answers [14 marks]

a) Show the truth table of a 3 input X-NOR gate.

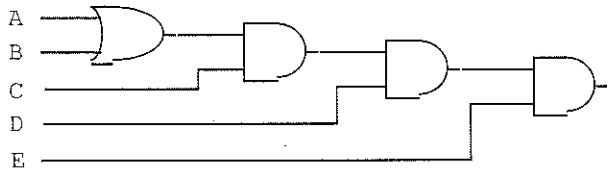
b) State the DeMorgan's theorems.

c) Convert decimal 64 to binary.

d) Convert the octal number 17_8 to decimal.

e) Convert the binary number 1001.00101 to decimal.

f) Derive the Boolean expression for the logic circuit shown below:



g) How many logic gates would be required to implement the following Boolean expression after simplification? $XY + X(X + Z) + Y(X + Z)$

Section C: Concepts and Designing [74 marks]

Question 1: Number Systems [13 marks]

a) Convert the decimal number 54.625 to binary. [4 marks]

b) Convert the decimal number -32480 to single-precision floating point binary number. [5 marks]

c) Convert the binary number 11000110 to Gray code. [2 marks]

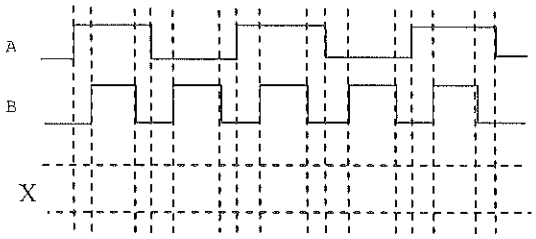
d) An even parity system receives the following code groups: 10110, 11010, 110011, 110101110100, and 1100010101010. Determine which groups, if any, are in error. [2 marks]

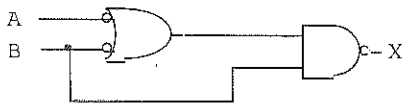
Question 2: Logic Gates and Boolean Algebra [25 marks]

a) Using Boolean algebra techniques and DeMorgan's theorems, simplify the expression $\overline{A}\overline{B}C + \overline{A + B + \overline{C}} + \overline{A}\overline{B}\overline{C}$ [3 marks]

Please Turn Over

b) Draw the output waveform for the two input system shown below with its proper time relationship to the inputs. (*Please answer on solution sheet provided*) [4 marks]





c) In a certain manufacturing plant, packets are being sorted into two groups according to their size, weight and colour. Only the packets with pre-specified size, weight and colour are retained while others are removed. Three separate sensors are used for these. The size and weight sensors produce a LOW level when the size and weight are above a specified level, while the colour sensor produces a HIGH when the specified colour is not detected. The packets to be retained are the ones that have their size or weight below the specified level and the colour is the given specified colour. Design a system that will indicate which packets are to be retained. Formulate the solution as follows:

i) Show the truth table for the problem solution. [2 marks]

ii) Determine the minimum SOP expression using Quine-McClusky's method. [4 marks]

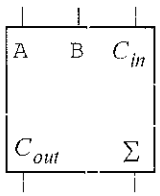
iii) Implement/draw the circuit using least number of logic gates. [2 marks]

d) Realize the function $Y = \overline{\overline{A}\,\overline{B}\,\overline{C} + D + E}$ using NOR gates only. [5 marks]

e) Realize the function $X = AB[C(\overline{DE} + \overline{AB})]$ using NAND gates only. [5 marks]

Question 3: Functions of Combinational Logic, MUX and DEMUX [14 marks]

a) Using the given basic block diagram of full adder, show how you will connect full adders to add 1101 and 1001. Show the inputs and outputs for each of the full adder. [4 marks]



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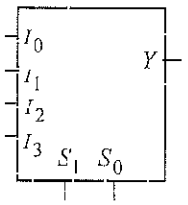
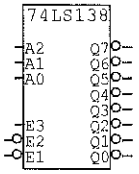
b) Realize the following Boolean equation using a 4-to-1 multiplexer. [6 marks]

$$f(A,B,C) = \sum_m (0,1,4,5,7)$$



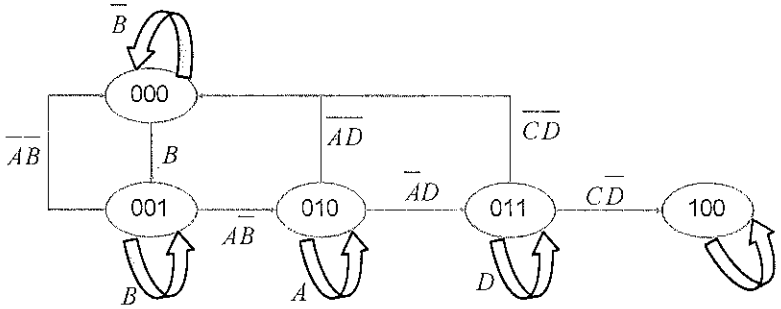
c) Implement the following function using a 3-to-8 decoder/demultiplexer. [4 marks]

$$f(A,B,C) = \sum_m (1,3,6,7)$$



Question 4: Flip-flops and Counters [12 marks]

a) Suppose you are selected as the design engineer for designing a synchronous digital lock system that has only four possible input keys (namely A, B, C, and D). The system is to produce a HIGH output only when the correct key sequence of BADC has been entered. If at any stage an incorrect sequence is entered/detected, the system should go to the initial state of zeros. The state diagram is given below. You are to utilize the state diagram given below and design the system (using T flip-flop) that will meet all the above requirements (plot the Karnaugh map, get the minimum expressions and implement the circuit). Note, the most significant bit is the bit controlling the lock. (Note: To keep the system simple, the next key is to be pressed before the current key is released in order for this system to work) [12 marks]



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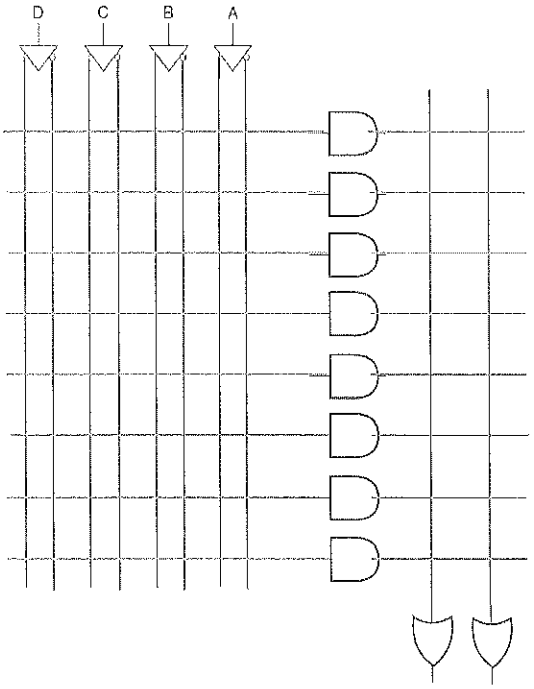
Question 5: Programmable Logic Devices [10 marks]

a) Show how the PLA given below should be programmed in order to implement the expression $Y = A\overline{B}C + \overline{A}B\overline{C} + \overline{A}\overline{B} + BC$. [3 marks]



b) Write the hardware description language (HDL) program for implementing a counter that will count in the sequence 0, 2, 1, 3 and repeat itself. You are to utilize ATF16V8BQL PLD programming. [7 marks]

THE END

ALL THE BEST FOR THE EXAMINATION

Please answer Section C; Q2 (b) and Q5 (a) on the solution sheet provided. Do not forget to attach this to your answer booklet.

Logic Design **EEE627**

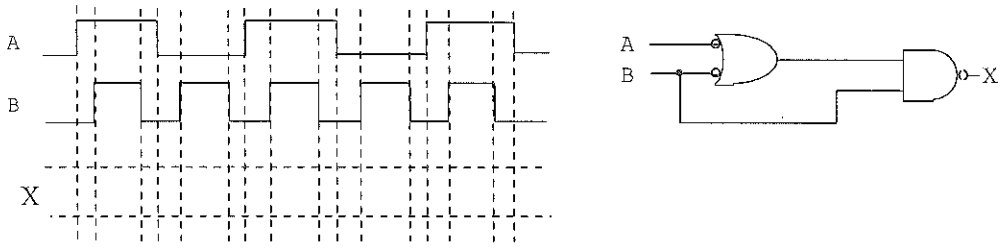
School of Electrical & Electronics Engineering
Fiji National University

Semester 1
2016

Final Examination – Solution Sheet

SOLUTION SHEET for Section C: Q2 (b) and Q5 (a). (Please attach this sheet to your Answer Booklet)

Section C: Question 2 (b)



Section C: Question 5 (a)