FNU FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

ADVANCED DIPLOMA IN ENGINEERING (ELECTRICAL & ELECTRONIC)

EEE604 – ELECTRO TECHNOLOGY(ELECTRONIC)
FINAL EXAMINATION – SEMESTER 1, 2016

DAY/DATE: 10/06/2016 TIME : 2.00 – 5.10PM
ROOM: TBA

INSTRUCTION TO STUDENT

1. You are allowed 10 minutes extra reading time during which you are NOT to write.
2. Begin each Question on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each answer & attached sheet.
4. Insert all written foolscaps, graph paper etc. in their correct sequence and secure with a string.
5. For all sheets of paper on which rough/draft work has been done, cross it through and you must attach all of them to your answer scripts.
6. Write clearly the number(s) of the question(s) attempted on the top of each sheet.
7. Tables & formula on the Appendix.
8. **SECTION A. - ATTEMPT ALL QUESTIONS**
9. **SECTION B. – SELECT TWO(2) QUESTION**
10. **SECTION C. – PICK ANY TWO(2) QUESTION**

SECTION - A: - Multiple Choice [15marks]

Choose only ONE correct answer from the choice given and use the Answer Sheet provided in your Answer Booklet.

(1) The field effect transistors (FET) are unipolar device, because...

(a) The current flow through it from biasing voltage.
(b) Biasing voltage is derived from the source.
(c) The current through it results from one of two kinds of charge carriers.
(d) Amplifies the voltage.

(2) The BJT Transistors is a bipolar device, because..?

(a) The current flow through it from biasing voltage.
(b) Biasing voltage is fixed by the potential divider connected to the base.
(c) Reverse breakdown voltage
(d) The current through it results from both kinds of charge carriers

(3) In a Sequential Logic Circuits, synchronous system does

(a) Create two terminal device used to vary the current in the circuit
(b) Sampled output at a definite instant time.
(c) Affect the output to propagates throughout the system.
(d) Create two terminal device used for storing voltage.

(4) Choose the correct statement which defines Asynchronous System.

(a) Two terminal device used to vary the current in the circuit
(b) Circuit responds to changes at the input at any time.
(c) A two terminal device that resist the flow of current.
(d) Do have common clock.

(5) Choose one of the disadvantages of the Synchronous system?

(a) Clock signals to be distributed only to few flip flops.
(b) Types of clock for controlling the system.
(c) Clock signals to be distributed only to every flip flops
(d) Clock signals is a high frequency signal.

(6) Why do Class A Amplifiers are not used for Power design?

(a) Tends to generate a lot heat energy.
(b) High theoretical efficiency of $\pi/4$
(c) Used for signal conditioning
(d) Low distortion and inefficient.

(7) What is one of the main characteristics of the counters?

(a) Remembers its past states
(b) All memory elements are triggered simultaneously
(c) Limits number of flip-flops used
(d) determine the number of states and the sequence.

(8) What is the purpose of *Oscillator* in an electronic system?

(a) inverts dc to ac voltage
(b) generator of sine-wave signal
(c) blocks ac voltages and allow dc voltage
(d) generator of square -wave signal

(9) In designing Oscillators, there two things which must be achieved before the oscillator will oscillate?

(a) biasing voltage and loop gain
(b) phase shift and high gain.
(c) unity loop gain and phase shift .
(d) low gain and phase angle

(10) Select the best type of filters which *System Power Supplies* often use?
(a) High Pass Filters
(b) Low Pass Filters
(c) Band stop filters.
(d) Band rejection filters

(11) Select the filter model type which used in *Anti-Aliasing Filter in Data converter* applications?

(a) Butterworth Low Pass Filters
(b) Butterworth High Pass Filters
(c) Tschebyscheff Low Pass Filters
(d) Tschebyscheff High Pass Filters.

(12) Name the passive component not included in the Clapp Oscillator configuration

(a) capacitors
(b) resistors
(c) inductors
(d) diodes.

(13) Approximately, what is the efficiency of a Class C amplifier?

(a) 50%
(b) 70%
(c) 90%
(d) 25%

(14) In designing Digital Circuit, which of the following device you will need to display the number you pressed on the keypad after releasing your finger?

(a) Decoder
(b) Encoder.
(c) Latching circuit.
(d) Multiplexor

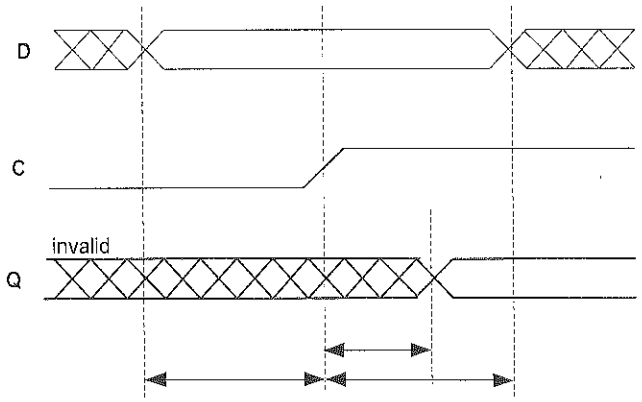
(15) Which Amplifier type which generates PWM output for its train pulses having width that are proportional to the level of the amplifier's input?

(a) Class A.
(b) Class B.
(c) Class C.
(d) Class D.

SECTION - A: SHORT ANSWERS (5 marks)

1. Describe the device that is used to store the data input in digital circuits. [2 marks]

2. Label the timing characteristics of the edge-triggered register. [3 marks]



SECTION - B: Optional Section **Answer <u>any 2</u> Question from this section.**

Question - 1 Oscillator Design

The gain of a certain oscillator system in fig.1 below as a function of frequency is $A(j\omega) = -16 \times 10^6/j\omega$. A feedback path connected around it has $\beta(j\omega) = 10^3/(2 \times 10^3+j\omega)^2$.

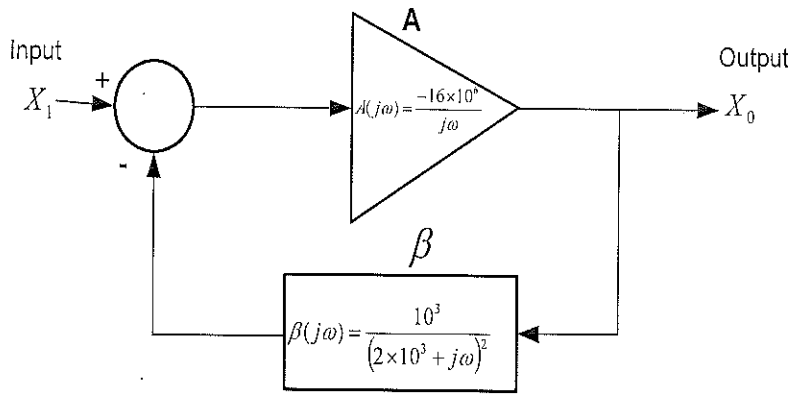


Fig.1 - Oscillator system

(a). Use Rectangular or Polar form to determine if the system will oscillate. (16 marks)
(b). Determine if your oscillator design will work, what will be the frequency that your oscillator will operate? (4 mark)

[20 marks]

Question – 2: 2nd Order LP Filter Design

Using the coefficient table attached at the back, design and draw an Active Second Order unity-gain Tschebyscheff Low-pass Filter with a cut-off frequency of 7kHz and a 3-dB passband ripple with C1= 22nF.

[20 marks]

Question 3 FET Amplifier Application

An NMOS inverter in the figure -2 below has the following parameters: $V_{T1} = V_{T2} = 2v$. $\beta_1 = 0.45 \times 10^{-3}$, $\beta_2 = 0.045 \times 10^{-3}$ and $V_{DD} = 12v$.

Determine the *high* and *low* output voltage.

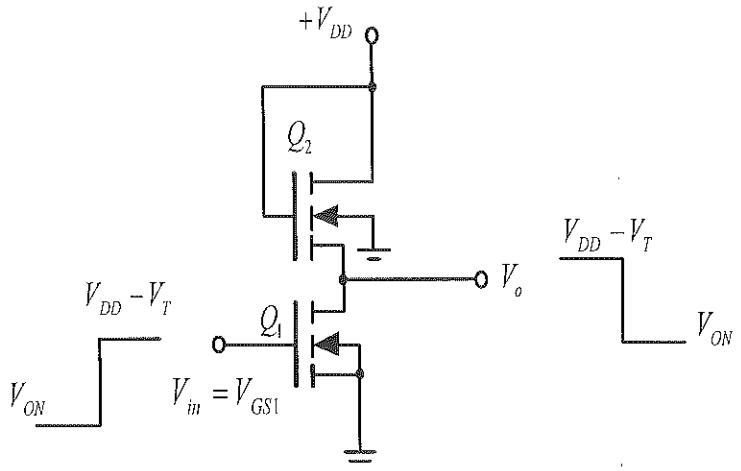


Fig.2 - NMOS Inverter Switch

[20 marks]

Question - 4 Multiplexer & Registers Design

(a) In the address decoding circuit in figure-8 below for a 4 x 8-bit shift register with an address decoder.

(i) Write down the Truth table for the system.
(ii) Write down the address combination which will select the following register C, A, D, B?
(iii) How many output will the five input decoder have?
(iv) Referring to part (iii), write down the truth table.

[10 marks]

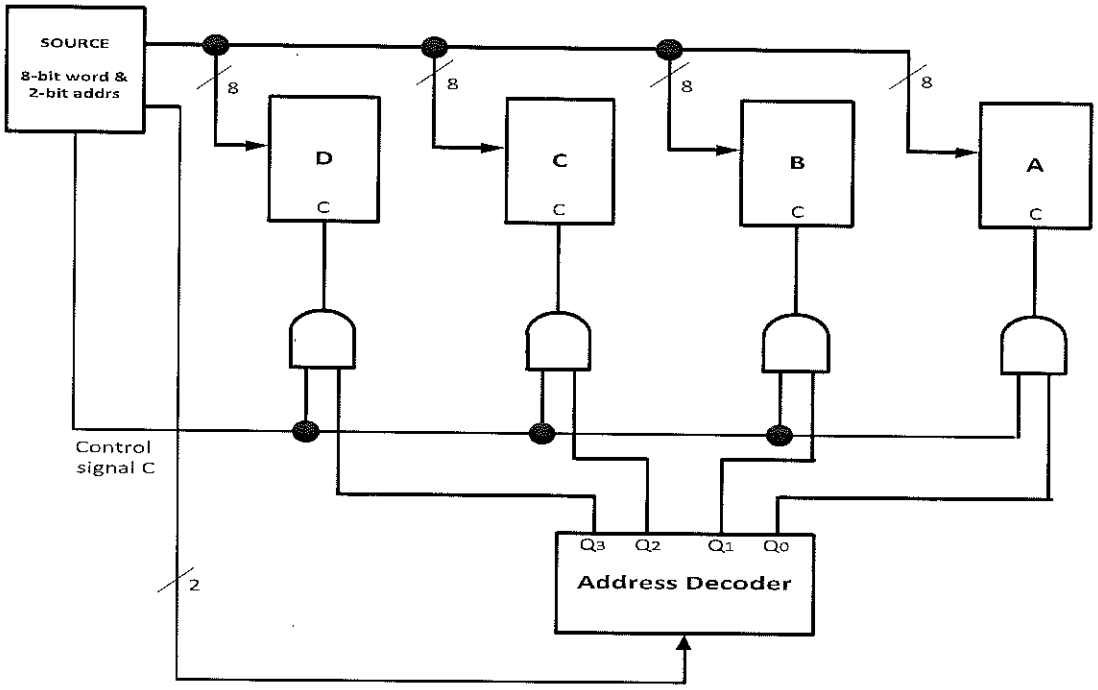


Figure-8: 2-Line Address decoder.

(b) Design and draw a Serial-In Parallel-out Shift Register using D type Flip flop that will do the following:-

(i) Receive the following serial data 101101001 in its input.
(ii) The clock circuit is common, to trigger in its trailing edge.
(iii) Draw its Timing Diagram for the next 10 clock pulse.
(iv) Explain the main effect of using Asynchronize clock circuit

[10 marks]

[20 marks]

SECTION - C: Answer any 2 Question from this section.

Question - 1 Series-Fed Class-A Amplifier

Referring to figure 4 below, an input voltage (V_{in}) in a base current of 10mA peak produces the characteristics shown in fig. 3(b) for a series-fed Class A amplifier. Calculate the following:-

(i)	Input Power	(4 marks)
(ii)	Output Power	(4 marks)
(iii)	Efficiency of Amp	(4 marks)
(iv)	Power dissipated by the transistor	(4 marks)
(v)	Identify advantages and disadvantages of negative feedback.	(4 marks)

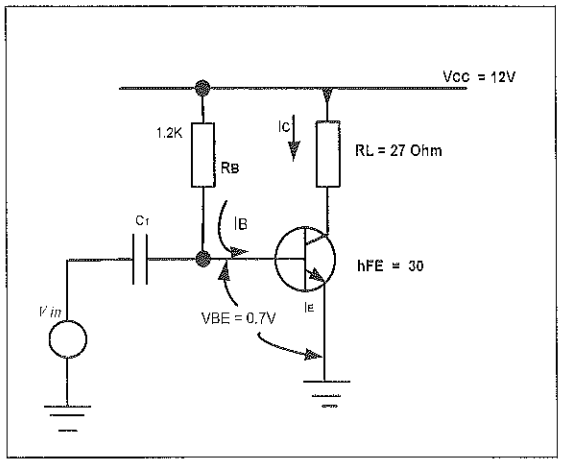


Fig.3a – Series-fed Class A Amplifier

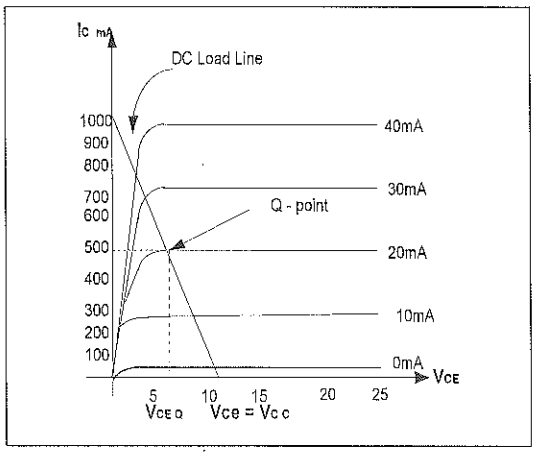


Fig.3b – Series-fed Class A characteristics graph

[20 Marks]

Question 2: Class C Power Amplifier

Fig.4 below shows a class C Power Amplifier with base bias voltage of -6v and V_{CC} = 30v. It is determined that a peak input voltage of 8.6V at 1 MHz is required to drive the transistor to its saturation current of 1.7A

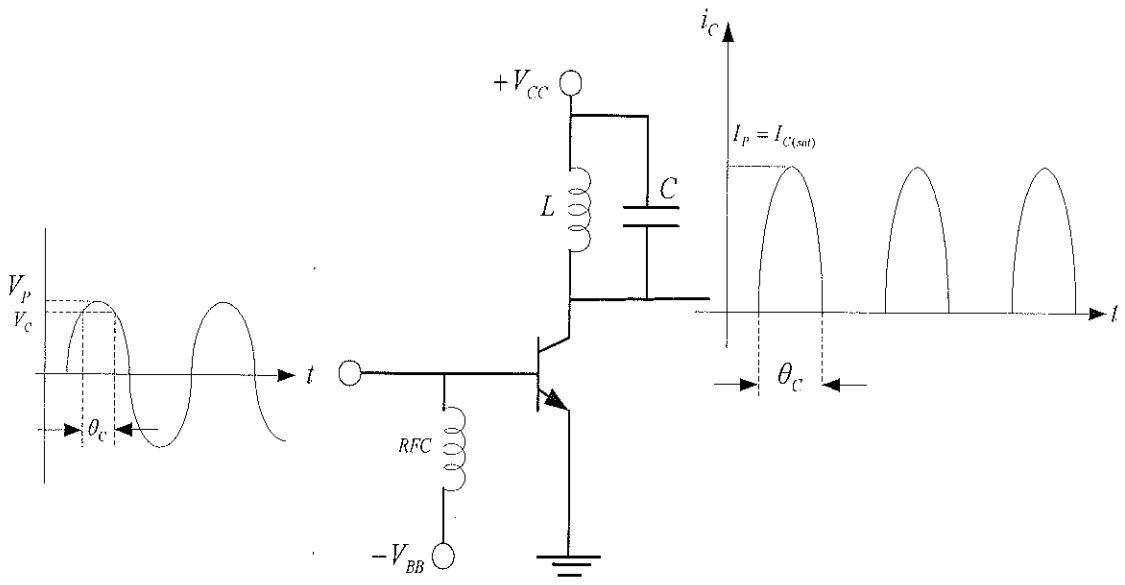


Fig.4 – Class C Power Amplifier

. Determine the following:-

(a). Amplifier's conduction angle. (5 marks)

(b). Amplifier's output power at 1MHz. (5 marks)

(c). Amplifier's efficiency. (4 marks)

(d). If the LC tank circuit having C = 470pF is connected in the collector circuit, find the inductance necessary to tune the amplifier.

(6 marks)

[20 marks]

Question 3: General Amplifier's Characteristics

(a) Clearly state all advantages and disadvantages of positive feedback.

[3 marks]

(b) Explain with aid of diagram the effect of increasing V_{DS} in N-Channel JFET, while gate is shorted to source, $V_{GS} = 0$.

[7 marks]

(c) Find the output voltage of the amplifier shown in figure 5 below, assuming that $r_s = 22\Omega$.

[10 marks]

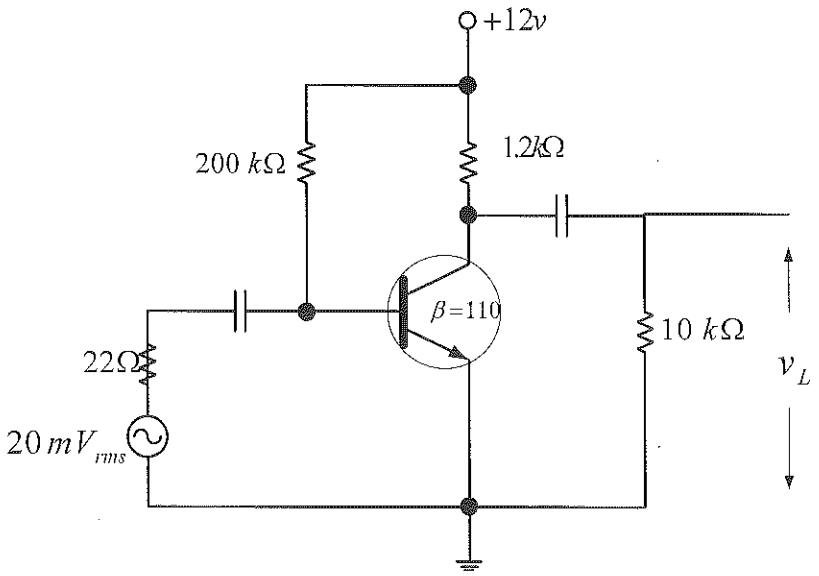


Fig. 5 - Common Emitter BJT amplifier

[20 marks]

Question - 4 Digital System Design & OP amps

(a) Figure 6 below shows a 4-bit synchronous shift register with Q_D output connected back to the DA input via an inverter. Assuming the initial state of the register is 0101.

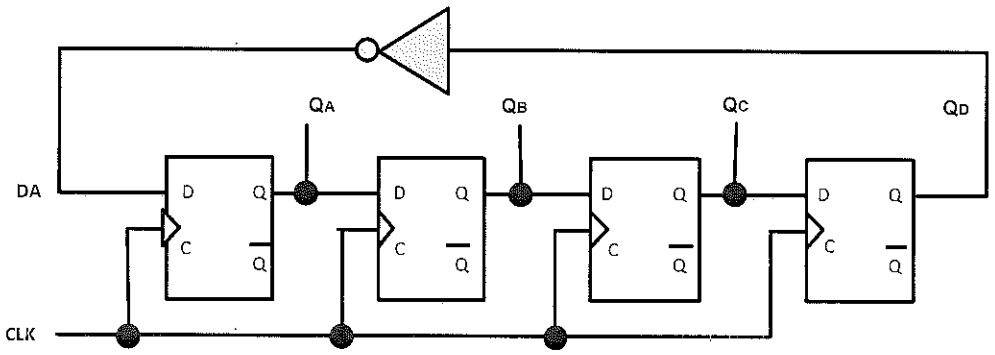


Figure-6: 4-bit Shift Register.

Give a brief account of how the above system works and produce the timing diagram for the output Q_A to Q_D for the next 10 clock pulses, before the output are repeated. **[10 marks]**

(b) In a non-inverting circuit in figure-7 below, the input resistance r_{in} of the op amp on its own is 110kΩ and the voltage gain Av of the Op amp is 210,000. **[6 marks]**

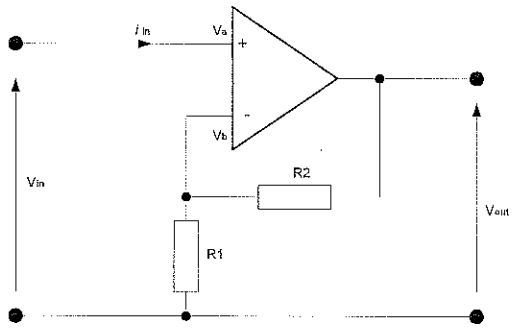


Fig.7 - Non- Inverting Amplifier

Calculate the overall gain G, and the input resistance R_{in} of the circuit above when:-

(i) R_1 = 1KΩ and R_2 = 40KΩ.
(ii) R_2 = 0
(iii) R_1 = 0KΩ and R_2 = 40KΩ.

(c) Briefly explain the applications, advantages & disadvantages of class-B amplifier system.

[4 marks]

[20 marks]

----------THE END ----------

Appendix 1

Formulas

1. $\frac{1}{2}\beta_2[(V_{DD}-V_{ON})-V_T]^2$, $\beta_1\left[(V_{DD}-2V_T)V_{ON}-0.5^2{}_{ON}\right]$

2. $Ai=\frac{hfe}{1+hoe.\,R_L}$ $A_P=6\left(\frac{D}{\lambda}\right)^2$

3. $C_2=C_1\frac{4b_1}{a_1{}^2}$ $P_Q=\left(\frac{2}{\pi^2}\times\frac{Vcc^2}{R_L}\right)\Big/2$

4. $K_OK_D=\frac{33.6f_O}{V_C}$ $X_1=\frac{a_1C_2\pm\sqrt{(a_1C_2)^2-4b_1C_1C_2}}{4\pi f_eC_1C_2}$

5. $X_C=\frac{1}{2\pi fC}$ $X_L=2\pi fL$ $P_{i(DC)}=V_{CC}.\left(2/\pi.Vcc/R_L\right)$

6. $f=\frac{1}{2\pi\sqrt{6}RC}$ $I_D=\beta V_{DS}\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)$

7. $Av=\frac{Vo}{Vi}=\left[hre-\frac{hie}{hfe}\left(\frac{1+hoe.R_L{}'}{R_L{}'}\right)\right]^{-1}$ $I_D=\frac{\beta(V_{GS}-V_T)^2(1+\lambda V_{DS})}{2}$

8. $I_B=\frac{Vcc-0.7v}{R_B}$, $I_C=h_{FE}.I_B$, $Vce=Vcc-IcR_L$

9. $I_D=I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$, $\beta_1\left[(V_{DD}-2V_T)V_{ON}-0.5^2{}_{ON}\right]$

10. $f_H=\pm\frac{8\,fo}{Vc}$, $V_{DS}=V_{DD}-I_DR_D$

Appendix 2

Filter Coefficients

SECOND-ORDER	BESSEL	BUTTERWORTH	3-dB TSCHEBYSCHEFF
a_1	1.3617	1.4142	1.065
b_1	0.618	1	1.9305
Q	0.58	0.71	1.3
R_4/R_3	0.268	0.568	0.234

. Second-Order Filter Coefficients

Tschebyscheff Coefficients

n	i	a_i	b_i	$k_i = f_{Ci} / f_C$	Q_i
1	1	1.0000	0.0000	1.000	—
2	1	1.3614	1.3827	1.000	0.86
3	1	1.9638	0.0000	0.537	—
	2	0.0640	1.1931	1.335	1.71
4	1	2.6282	3.4341	0.538	0.71
	2	0.3648	1.1509	1.419	2.94
5	1	2.9235	0.0000	0.342	—
	2	1.3025	2.3534	0.861	1.16
	3	0.2290	1.0933	1.460	4.54
6	1	3.9645	6.8797	0.366	0.68
	2	0.7528	1.9573	1.076	1.61
	3	0.1589	1.0711	1.495	6.51
7	1	4.0211	0.0000	0.249	—
	2	1.9729	4.1795	0.645	1.09
	3	0.4961	1.5676	1.206	2.58
	4	0.1156	1.0443	1.517	8.84
8	1	5.1117	11.980 7	0.276	0.68
	2	1.0839	2.9365	0.844	1.61
	3	0.3439	1.4208	1.264	3.47
	4	0.0885	1.0407	1.521	11.53
9	1	5.1318	0.0000	0.195	—
	2	2.4283	6.6307	0.506	1.06
	3	0.6839	2.2908	0.989	2.21
	4	0.2559	1.3133	1.344	4.48
	5	0.0695	1.0272	1.532	14.66
10	1	6.3548	18.369 5	0.222	0.67
	2	1.3582	4.3453	0.689	1.53
	3	0.4822	1.9440	1.091	2.89
	4	0.1994	1.2520	1.381	5.61
	5	0.0563	1.0263	1.533	17.99

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