FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

DIPLOMA IN ELECTRICAL & ELECTRONIC ENGINEERING

EEE502 – DIGITAL ELECTRONICS 2B.

FINAL EXAMINATION - SEMESTER 1 - 2016.

DURATION OF EXAM: 3HOURS

INSTRUCTIONS TO STUDENTS:

1. You are allowed 10 minutes **EXTRA** as reading time during which you are **NOT** to write.
2. Total Number of pages: 8 pages. [Pages 1 – 8]
3. Begin each answer on a fresh page and use both sides of the sheet.
4. Write your candidate number at the top of each attached sheet.
5. Insert all written foolscap, graph paper, drawing paper, etc. in their correct sequence and secure well.
6. For all sheets of paper on which rough/draft work has been done, cross it through and attach to your answer scripts.
7. Show all workings where necessary
8. Diagrams and graphs can be drawn in pencil.
9. Non- programmable calculators are allowed.
10. **Attempt all questions in Sections A B, C, D & select one question from 3 in Section E.**
11. **Check your work before you leave the room!!**

Section A: **[20 marks]**

Q1. Arithmetic Circuits

a) Given the binary equivalent of 45 as 101101, write its 1's and 2's complement

b) How do you represent this number as a positive number?

c) How do you represent this number as a negative number?

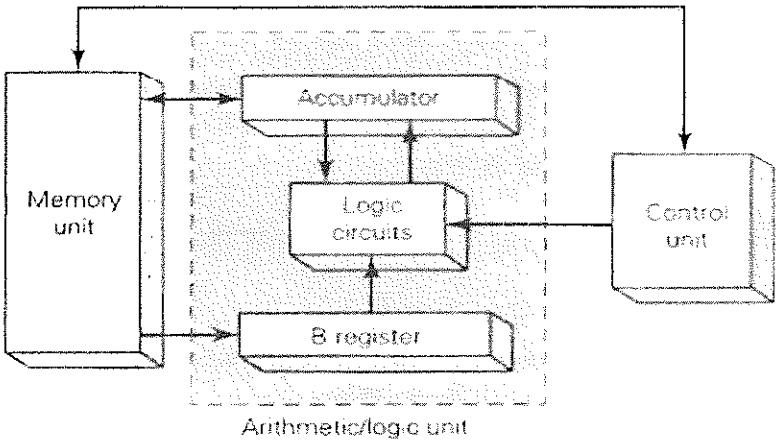
(6 marks)

Q2.

a) Write a function table for a half adder (inputs A and B, outputs SUM and CARRY). **(4 marks)**

b) From the function table, design a logic circuit that will act as a half adder. **(4 marks)**

c) The figure below shows a block diagram showing the major elements of a typical Arithmetic Logic Unit (ALU).



Briefly explain a typical sequence of operation that may occur in an ALU. **(6 marks)**

Section B: **[20 marks]**

Q1. Memory Devices

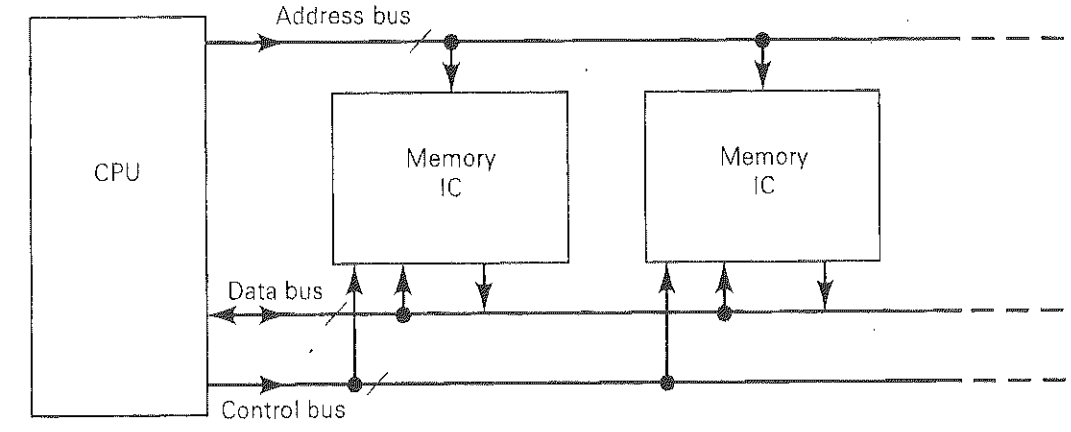
a) Define the following terminologies in relation to Memory Devices:

i) Access Time
ii) Volatile Memory
iii) Address
iv) Random Access Memory (RAM)
v) Read Only Memory (ROM) **(2 marks each)**

b) The figure below depicts the interfacing of Memory ICs (RAM & ROM) to the CPU over the three groups of signal lines or buses.

i) List down the function of the address lines

ii) Outline the 5 steps that take place when the CPU reads from memory.

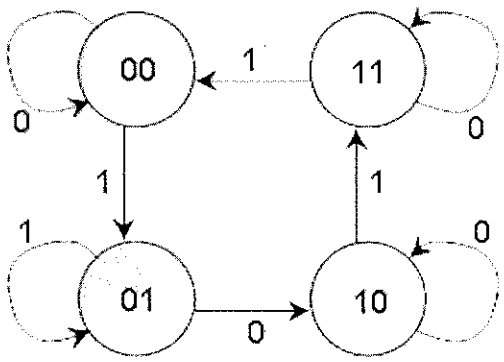


(10 marks)

Section C **[30 marks]**

Q1. Sequential Circuit Design

a) Using JK Flip Flops, design a Synchronous sequential circuit whose state diagram is shown below. Break down your solution into the following steps:



i) Derive the Circuit Excitation Table from the state diagram

ii) Derive the characteristic table for JK Flip Flop and hence its excitation table

iii) Derive the excitation table for the circuit; ie (Present state, Next state, Inputs and flip flop Inputs)

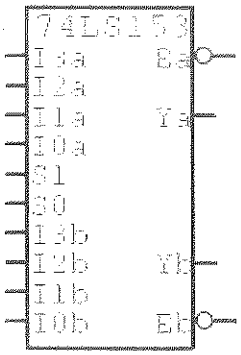
iv) From the K-map derive the output variables of the jK flip flops.

v) Design the logic circuit needed to generate the levels required at each J and K input

Section D **[20 marks]**

Q1. Decoder & Multiplexer

a) Using the 74LS153 Dual 4-to-1 Multiplexer shown below, realize the Boolean functions, f_1 = (C, B, A) = $\sum_m(0,1,6,7)$ and f_2 = (C, B, A) = $\sum_m(1,2,3,5)$ so that only one output is present at any one time, i.e. either f_1 or f_2 only, and not both. Note that the 74LS153 has an "Enable" control line. (Datasheet for the 74LS153 is attached).



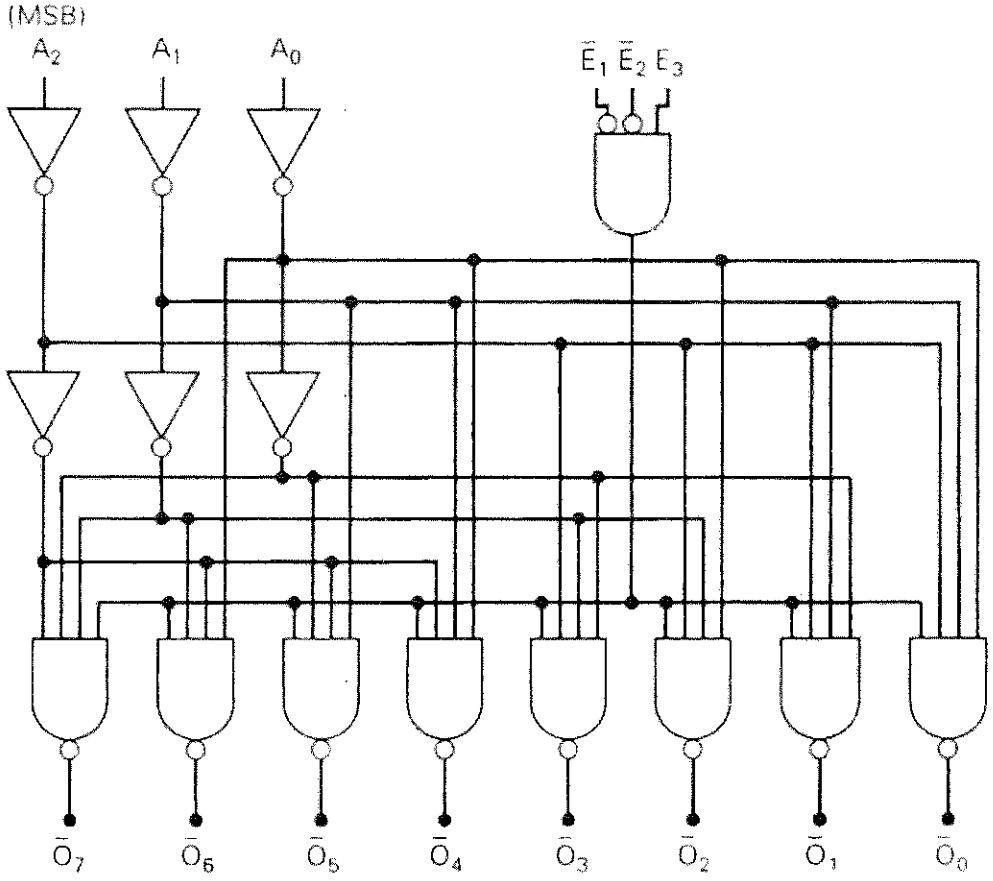
(10 marks)

b) Shown below is a logic circuit of a 74ALS138 decoder; its truth table and its logic symbol. Indicate the state of the 74ALS138 output for each of the following set of inputs:

i) E3 = 1; E2 = E1 = 0; A2 = 0, A1 = A0 = 1.

ii) E3 = E2 = E1 = 1; A2 = A1, A0 = 1

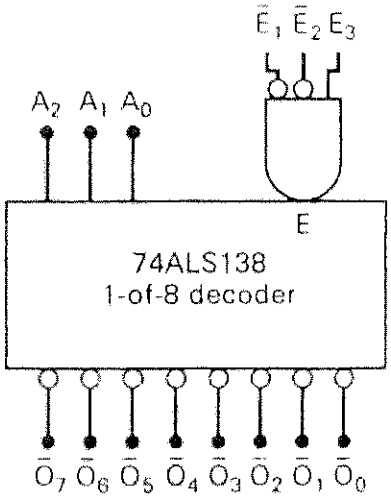
iii) E3 = E2 =E1 =0, A2 =A1 =A0 =0



(a)

$\bar{E}_1$	$\bar{E}_2$	E_3	Outputs
0	0	1	Respond to input code $A_2A_1A_0$
1	X	X	Disabled – all HIGH
X	1	X	Disabled – all HIGH
X	X	0	Disabled – all HIGH

(b)



(c)

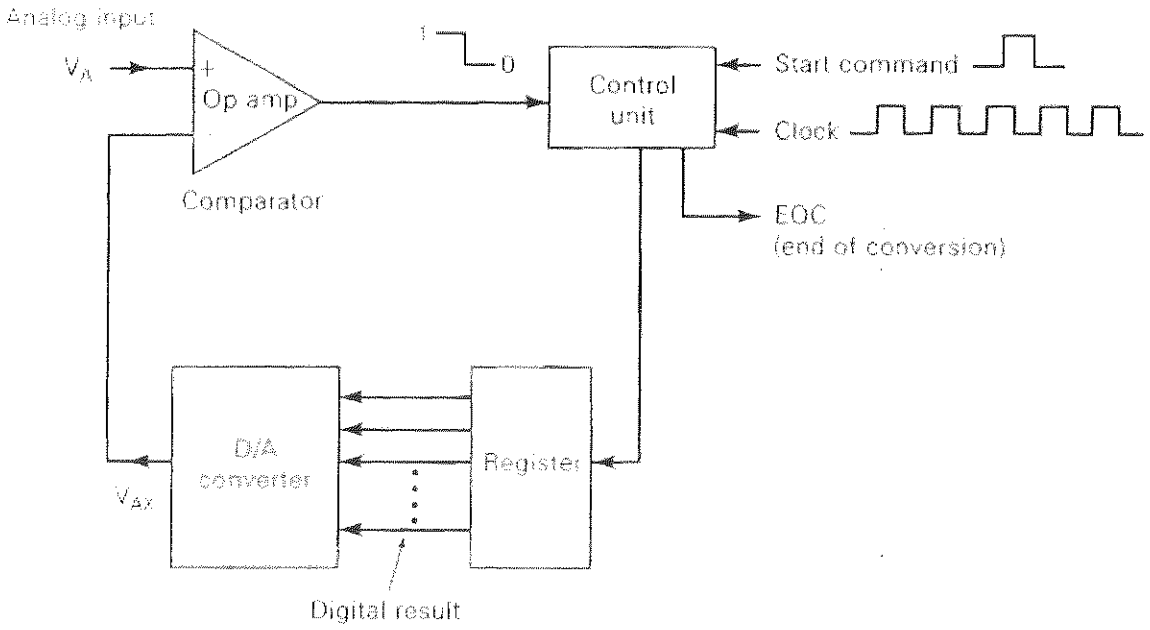
(10 marks)

Section E: Select One Question only from the 3 below

[10 marks]

Q1. Analog to Digital Conversion & Counters

a) The figure below depicts a block diagram of an Analog to Digital Converter (ADC). Describe in your own words how the analog input V_A is converted to its digital output equivalent.



(10 marks)

Q2. PLA.

a) Explain what a "Programmable Logic Array" (PLA) is and its use.

b) Given the truth table shown below, write the Boolean expression in SOP form and program the PLA. The Xs are the 3 inputs where X_0 is the lowest significant bit (LSB); and X_2 the most significant bit (MSB); and the Ys are the outputs.

X_2	X_1	X_0	Y_1	Y_2
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	1	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	0	1

(10 marks)

Q3. Design of Asynchronous and Synchronous Counter

Using JK Flip Flops, design a Synchronous Modulo 5 Counter that counts in the sequence: 0, 1, 2, 3, 4 and back to 0. Break down your solution into the following steps:

i) Develop the State Transition Diagram

ii) Derive the Circuit Excitation Table

iii) Implement the final expression from the K-map

(10 marks)

----------THE END----------