



COLLEGE OF ENGINEERING, SCIENCE & TECHNOLOGY (CEST)

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

TRADE DIPLOMA IN ELECTRICAL ENGINEERING

(ELECTRICAL AND RENEWABLE ENERGY) – STAGE 3

EEE437- INTRODUCTION TO ELECTRONICS

FINAL EXAMINATION – SEMSTER 1, 2016

INSTRUCTIONS TO STUDENTS

1. *You are allowed 10 minutes Extra reading time during which you are NOT to write.*
2. *Begin each answer on a fresh page and use both sides of the sheet.*
3. *Write your candidate-number at the top of each attached sheet*
4. *Insert all written foolscaps, graph paper, drawing paper, etc. in their correct sequence and secure with string*
5. *For all sheets of paper on which rough/draft work has been done, cross it through and you MUST ATTACH to you answer scripts.*
6. *Write clearly the number(s) of the question(s) attempted on the top of each sheet.*
7. **ANSWER ALL QUESTIONS.**
8. *Show all workings where necessary.*
9. *Do not use programmable calculators.*
10. **ALWAYS CHECK YOUR WORK BEFORE YOU LEAVE THE ROOM!**

Section A**Multiple Choice****[30 Marks]**

Circle correct letter (A, B, C or D) against each of numbers 1 through 30.
Remove and attach to your Answer Booklet.

- 1. The binary number 1101 is equal to the decimal number**
 - A. 13
 - B. 49
 - C. 11
 - D. 3

- 2. The sum of 11010 + 01111 equals**
 - A. 101001
 - B. 101010
 - C. 110101
 - D. 101000

- 3. The ASCII code is?**
 - A. A positional value code.
 - B. A minimum change code.
 - C. An Alphanumeric code.
 - D. A straight binary code.

- 4. Which of the following is a forbidden code group in BCD?**
 - A. 0010
 - B. 0101
 - C. 1000
 - D. 1011

- 5. An Ultra Large Scale Integration (ULSI) device has a circuit complexity of**
 - A. 12 to 99 equivalent gates
 - B. Over 100,000
 - C. 2000 to 5000 equivalent gates
 - D. 100 to 9999 equivalent gates

- 6. A 5 – bit binary counter has a maximum modulus of**
 - A. 16

- B. 32.
C. 8
D. 4
7. **According to De-Morgan's theorem, which of the following equality(s) are correct?**
- A. $\overline{A B} = \overline{A} + \overline{B}$
B. $\overline{XYZ} = \overline{X} + \overline{Y} + \overline{Z}$
C. $A + B + C = \overline{A B C}$
D. all of the above
8. **A logic**
- A. two AND gates and one OR gate
B. two AND gates and one OR gate and one inverter
C. two OR gates and one AND gate and two inverters
D. two AND gates and one OR gate and two inverters
9. **An inverter performs an operation known as**
- A. conversion
B. assertion
C. complementation
D. both (A) and (C)
10. **Asynchronous counters are known as**
- A. ripple counters
B. multiple clock counters
C. decade counters
D. modulus counters
11. **A pulse is applied to each input of a 2 – input NAND gate. One pulse goes HIGH at t=0 and goes back LOW at t = 1ms. The other pulse goes HIGH at t = 0.8ms and goes back LOW at t=3ms. The output pulse can be described as follows:**
- A. It goes LOW at t=0 and back HIGH at t=3ms
B. It goes LOW at t=0.8ms and back HIGH at t=3ms
C. It goes LOW at t=0.8ms and back HIGH at t=1ms
D. It goes HIGH at t=0.8ms and back LOW at t=3ms

12. The group of bits 11101110 is serially shifted (right most bit first) into an 8 bit parallel output shift register with an initial state of 10101110. After three clock pulses, the register contains.

- A. 01011110
- B. 10110101
- C. 00101101
- D. 11010101

13. To measure the period of a pulse waveform, you must use

- A. a DMM
- B. an Oscilloscope
- C. a Logic probe
- D. A pulser

14. In an R/2R DAC, there are

- A. four values of resistors.
- B. One resistor value
- C. Two resistor values.
- D. A number of resistor values equal to the number of inputs.

15. An 8-bit DAC has a resolution of

- A. 0.1%
- B. 0.392%
- C. 1%
- D. 3.92%

16. The type of analog-to-digital converter(ADC) with the fastest conversion time is

- A. flash
- B. digital ramp
- C. tracking
- D. simultaneous conversion

17. The TTL family with the fastest switching speed is?

- A. Standard TTL
- B. ALS
- C. S
- D. AS

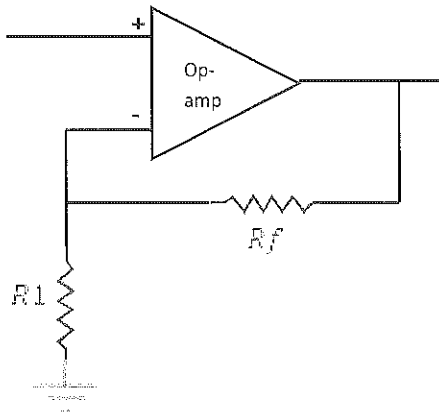
18. To implement the expression $ABCD + ABCD + ABCD$, it takes one OR gate and

- A. One AND gate
- B. Three AND gates
- C. Three AND gates and four inverters
- D. Three AND gates and three inverters

19. How many layers does a transistor have?

- A. 1
- B. 2
- C. 4
- D. 3

20. Calculate the overall voltage gain of the circuit if $R_1 = 200\Omega$ and $R_f = 2k\Omega$



- A. -1
- B. -10
- C. 9

D. 11

21. What is the slew rate of an op-amp if the output voltages change from 3 V to 6 V in 0.3ms?

- A. 5 V/ms
- B. 10 V/ms
- C. 2 V/ms
- D. 1 V/ms

22. If $A_v(d) = 300$ and $A_{cm} = 0.06$, the CMRR is

- A. 625
- B. 5,000
- C. 80dB
- D. 18

23. Which of the following pin numbers represent the inverting input of LM741 operational amplifier?

- A. 2
- B. 3
- C. 4
- D. 6

24. In NPN transistor, the P-Region are

- A. Base and emitter
- B. Base and collector
- C. Emitter and collector
- D. Only base

25. If I_c is 50 times larger than I_B , then β is

- A. 0.02
- B. 100
- C. 50
- D. 500

26. What is the output voltage of the fixed regulator type?

7812

- A. -24 V
- B. +12 V
- C. +79 V
- D. -92 V

27. BJT is a _____ controlled device. The JFET is a _____ controlled device

- A. Voltage, voltage
- B. Voltage, Current
- C. Current, Voltage
- D. Current, Current

28. A JFET always operates with

- A. The gate-to-source *pn* junction reversed-biased
- B. The gate-to-source *pn* junction forward-biased
- C. The drain connected to ground
- D. The gate connected to source

29. For a properly biased PNP transistor, let $I_C=15\text{mA}$ and $I_E=15.3\text{mA}$. what is the level of I_B ?

- A. 0.3A
- B. $300\mu\text{A}$
- C. 300mA
- D. 30.2mA

30. When operated in active region, the transistor acts like

- A. A linear amplifier
- B. A switch
- C. A variable capacitor
- D. A variable resistor

SECTION B

[70 Marks]

PART I - DIGITAL ELECTRONICS

QUESTION 1 (10 Marks)

- a) With aid of diagrams explain the difference between **Analogue quantities** and **Digital quantities.** (2 marks)
- b) Determine the decimal value of the binary number 1101101_2 . (1 mark)
- c) Convert 234_{10} to BCD (1 mark)
- d) What is the binary representation for 72_{10} (2 marks)
- e) Convert hexadecimal number $A3_{16}$ to decimal number (2 marks)
- f) Convert the decimal number 241_{10} to Excess – 3 codes. (2 marks)

QUESTION 2 (15 MARKS)

- a) Refer to diagram in **Figure – 2a** below to answer questions;
 - i. Sketch the truth table **(5 marks)**
 - ii. Write the logic equation of output Q **(2 marks)**

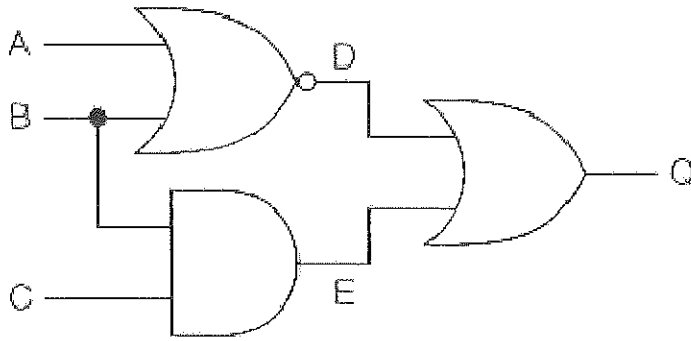


Fig 2 - a

- b) Using Boolean algebra techniques to simplify this expression:

$$AB + A(B + C) + B(B + C)$$

(5 marks)

- c) Apply De Morgan's theorem to the expression below:

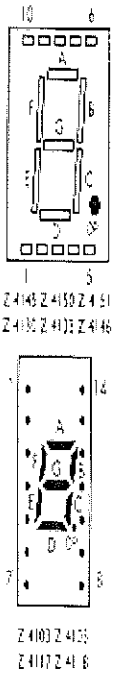
$$\overline{(\overline{A} + B) + CD}$$

(3 marks)

QUESTION 3 (15 MARKS)

Use the data sheet where necessary to answer question below:

7-SEGMENT LEDs										
	LTS312AR Z 4117	LTS313AR Z 4103	LTS3303AR Z 4150	LTS5503AE Z 4151	LTS346AR Z 4145	LTS313AG Z 4105	30240A	LSD5115 Z 4118	LSD5114 Z-4130	LSD5365 Z4146
Characteristics										
Common Terminal Pol.	Anode	Cathode	Cathode	Cathode	Anode	Cathode	Anode	Cathode	Cathode	Anode
Digit Size	7.6mm	7.6mm	14.2mm	14.2mm	13.3mm	7.6mm	7.6mm	13.1mm	14.2mm	14.2mm
Colour	Red	Red	Red	Orange	Red	Green	Red	red	Orange	Red
An. Fwd. Seg. Current	25mA	25mA	25mA	25mA	25mA	25mA	25mA	25mA	25mA	25mA
Segment Voltage	1.7	1.7	1.7	2.1	1.7	2.1	2.0	1.7	2.0	1.7
Min. Rev. Bkdn. Volt.	5	5	5	5	5	5	5	5	5	5
Max. Rev. Current	100µA	100µA	100µA	100µA	100µA	100µA	100µA	10µA	10µA	10µA
Seg. Intensity (typ.)	450µcd	450µcd	500µcd	2000µcd	500µcd	2000µcd	750µcd	6000µcd	4500µcd	8500µcd
Max. Seg. Dissipation	55mW	55mW	55mW	75mW	55mW	75mW	85mW	110mW	100mW	110mW
Connections										
Seg. A	1	10	7	7	7	10	1	7	7	7
Seg. B	13	9	6	6	6	9	13	6	6	6
Seg. C	10	8	4	4	4	8	10	4	4	4
Seg. D	8	5	2	2	2	5	8	2	2	2
Seg. E	7	4	1	1	1	4	7	1	1	1
Seg. F	2	2	9	9	9	2	2	9	9	9
Seg. G	11	3	10	10	10	3	11	10	10	10
Dec. Pt.	9	7	5	5	5	7	6,9	5	5	5
Common	3,14	1,6	3,8	3,8	3,8	1,6	3,14	3,8	3,8	3,8



a) Calculate the value of the safety resistor to display a digit 3 using a Z 4117 display. **(2 marks)**

b) Figure – 3b below shows a four - bit Digital to Analog converter (DAC).

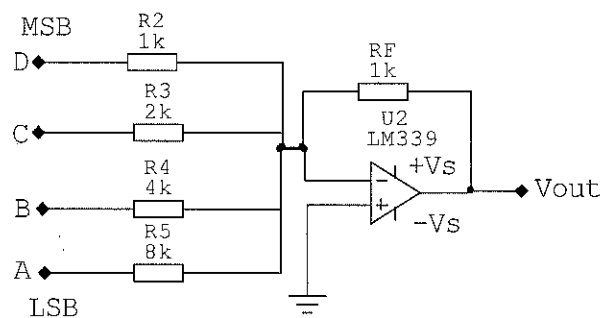


Fig – 3b

Calculate the output voltage (**V_{out}**) if the DCBA inputs are as follows respectively:

- i. 1101
- ii. 1001

(3 marks)

c) Show how NAND gates only are used to perform the function of a **two - input OR gate**. **(2 marks)**

d) Refer to the diagram in **Figure 3-d** below and answer the following questions.

i) What is the decimal output from the decoder that appears on the 7-segment display? **(1 mark)**

ii) If the BCD input is 0010, what segments will be illuminated? **(1 mark)**

iii) What special name is given to the resistors that are added between the decoder and the display? **(1mark)**

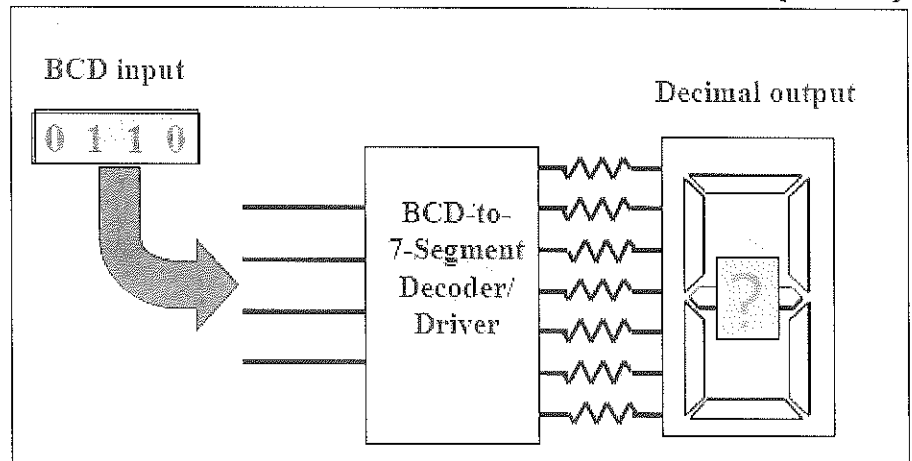


Figure 3-d

e) Refer to the table below and make your analysis on the three types of gates in terms of their speed, power consumption, noise margin, fan-in and fan-out. While comparing, state which one is best to use. **(5 marks)**

Type of Gate	Fan-in	Fan-out	Propagation delay (ns)	Noise margin (V)	Power consumption (mW)
TTL	8	10	9	0.4	40
CMOS	8	50	30	1.5	1
ECL	5	50	1.1	0.4	30

PART II - ANALOGUE ELECTRONICS

QUESTION 1 (15 Marks)

- a) Draw the standard symbol of both the NPN and PNP transistor. **(2 marks)**
- b) Use the **BJT Data Sheet** provided to answer the questions asked.

TYPE	CASE	POL MAT	V_{CE}	V_{CB}	$I_{C\text{ mA}}$	$V_{CES} @ I_{C\text{ mA}}$	$H_{fe} @ I_{C\text{ mA}}$	P(TOT) mW	USE	EQUIVALENT
BD140	TO-126	PS	80	100	1.5A	0.5@500	40@250	8W	G.P. o/p	40410
BC107	TO-18	NS	45	50	100	0.25@10	110@450	300	G.P.S.S. amp	BC207, BC147, BC182
BC559	TO-92 VAR 1	PS	30	30	100	0.65@100	125@800	500	G.P.S.S. amp	BC159
2N3055	TO-3	NS	60	70	15 A	1.1@4A	20@70 4A	115W	G.P. power	BDY 20
TIP 3055	TOP-3	NS	70	100	15 A	1.1@4A	20@ 4A	90W	Power output	MJE 3055

- i. Current gain of BC559 and what current can this transistor operate from? **(2 marks)**
- ii. Material used in all transistors? **(1 mark)**
- iii. Abbreviation of G.P.S.S. from the table. **(2 marks)**
- iv. Power dissipation of BC107? **(1 mark)**
- v. Package of TIP3055? **(1 mark)**
- vi. Polarity of the BC207 transistor? **(1 mark)**

c) Refer to the circuit in **Fig 1-c** below

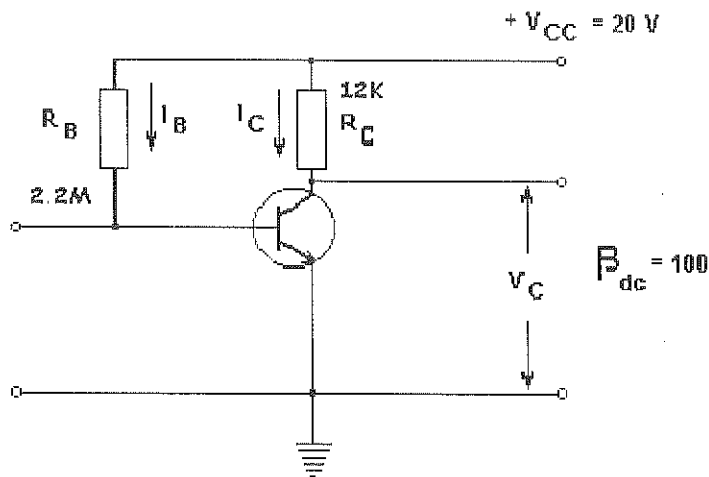


Fig 1-c

- Calculate the values of:
- i) I_B (2 marks)
 - ii) I_C (1 mark)
 - iii) V_C (2 marks)

QUESTION 2 [15 Marks]

- a) **Fig 2-E** shows a circuit of a **Junction Field Effect Transistor (JFET)**. It shows biased voltages applied to an N – Channel device.
Clearly explain the JFET Operation from the circuit below.

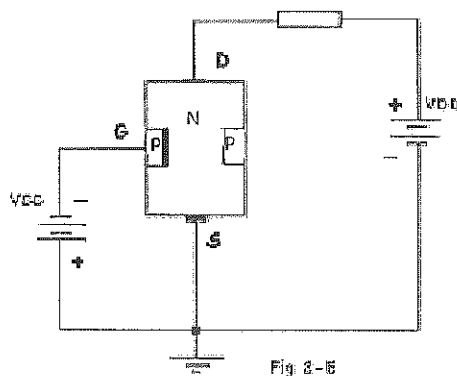


Fig 2-E

(3 marks)

b) Sketch the block diagram of **Basic DC power supply** and explain the function of each blocks. **(8 marks)**

c) **Fig 2-c** below shows a circuit diagram of an Op-Amp circuit.

i) Identify the circuit. **(1 mark)**

ii) Calculate the **output Voltage (V_o)**. **(3 mark)**

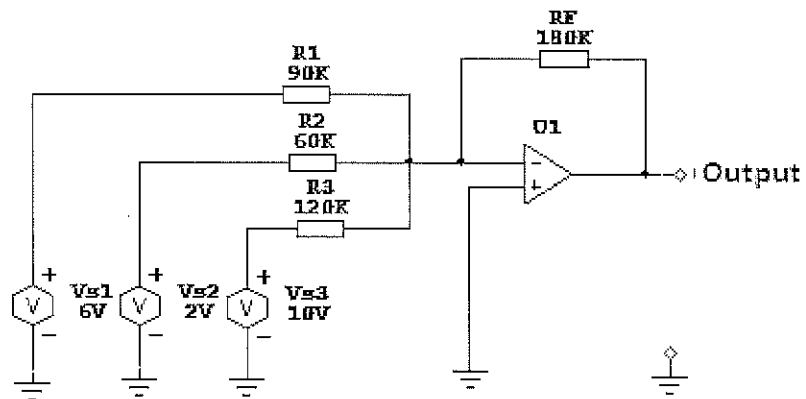


Fig - 2C

END OF THE PAPER

Candidate No:

Section A

Multiple-Choice Matrix

[30 marks]

Circle the correct letter (A, B, C or D) against each of numbers 1 through 30.

Remove and attach to your Answer Booklet.

1	A	B	C	D
2	A	B	C	D
3	A	B	C	D
4	A	B	C	D
5	A	B	C	D
6	A	B	C	D
7	A	B	C	D
8	A	B	C	D
9	A	B	C	D
10	A	B	C	D
11	A	B	C	D
12	A	B	C	D
13	A	B	C	D
14	A	B	C	D
15	A	B	C	D
16	A	B	C	D
17	A	B	C	D
18	A	B	C	D
19	A	B	C	D
20	A	B	C	D
21	A	B	C	D
22	A	B	C	D
23	A	B	C	D
24	A	B	C	D
25	A	B	C	D
26	A	B	C	D
27	A	B	C	D
28	A	B	C	D
29	A	B	C	D
30	A	B	C	D



Class Listing

School of Electrical & Electronics Engineering

Samabula

Semester1

2016

EEE437 Introduction to Electronics NL

StudentID	Name	Status	Mon	Sponsor	Outstanding Fee
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Trade Diploma in Electrical Engineering (Electrical and

2008002491	Basarat Ahmad Raza	EA			
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2008003923	Sailosi Madrai	EA			2,879.56
2013114834	Tony Ravula Ketewai	ER		- Full	53.00
		4			
				Total Owing:	2,932.56
	Total Count:	4		Grand Total:	2,932.56

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Instructions	/	
Total Number of Pages	/	
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ERRS (Class List)	/	
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