FNU FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE & TECHNOLOGY (CEST)

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

CERTIFICATE IV IN ELECTRONIC ENGINEERING

EEE412- DIGITAL ELECTRONICS 1A

FINAL EXAMINATION – PENSTER 2, 2016

DATE: As per timetable **TIME:** As per timetable

TIME ALLOWED: 2 HOURS

INSTRUCTIONS TO STUDENTS

1. *You are allowed 10 minutes Extra reading time during which you are NOT to write.*
2. *Begin each section on a new page and use both sides of the sheet.*
3. *Write your candidate-number at the top of each attached sheet.*
4. *Insert all written foolscaps, graph paper, drawing paper, etc. in their correct sequence and secure with string.*
5. *For all sheets of paper on which rough/draft work has been done, cross each one through and ATTACH these to your answer scripts.*
6. *Write clearly the number(s) of the question(s) attempted on the top of each sheet.*
7. *ANSWER ALL QUESTIONS.*
8. *Show all working clearly where necessary.*
9. *Programmable calculators are not allowed, especially the ones that does the conversions of number systems.*
10. ALWAYS CHECK YOUR WORK BEFORE YOU LEAVE THE ROOM!

Section A – Multiple Choice [20 marks]

Choose the appropriate answer from each question by writing the alphabet beside the question number in your answer booklet.

1. The SOP form of the Boolean expression A + B(D + CE) + F is;
   A. (A + B)(BCD + BEF)
   B. AB + BCD + BE + BF
   C. (A + B)(B + C + D)(B + E + F)
   D. A + BD + BCE + F

2. The binary number 1011 is equal to the decimal number
   A. 13
   B. 49
   C. 11
   D. 3

3. The decimal number 21 is equal to the binary number
   A. 10010
   B. 11000
   C. 10101
   D. 01001

4. The Boolean expression $A+\overline{B}+C$ is a;
   A. Sum term
   B. Literal term
   C. Product term
   D. Complemented term

5. What is the weight of digit 6 in the decimal number 1386?
   A. 1
   B. 2
   C. 3
   D. 0

6. The Boolean expression for a 4-input OR gate is;
   A. A + B + C + D
   B. ABCD
   C. AB + CD
   D. A + B x C + D

Please turn over

7. What is the total number of possible combinations of binary inputs to a gate having three input variables?
   A. 2
   B. 4
   C. 8
   D. 16

8. Determine the value of **C** that make the product term $A\overline{B}C\overline{D}$ equal to 1.
   A. 0
   B. 1
   C. 1010
   D. 0101

9. What does an exclusive OR (XOR) gate do?
   A. Gives a high output when one or more of its inputs are high.
   B. Gives a high output when only one of its inputs are high.
   C. Gives a low output when one or more of its inputs are high.
   D. Gives a low output when only one of its inputs are high.

10. The binary number for $E6A5_{16}$ is
   A. 1111011110101001
   B. 1110111110101001
   C. 1110011010100101
   D. 1111011010101001

11. How is a *J-K* flip-flop made to toggle?
   A. J = 0, K = 0
   B. J = 1, K = 1
   C. J = 1, K = 0
   D. J = 0, K = 1

12. Applying DeMorgan's theorem to the expression $\overline{ABC}$ will give;
   A. $\overline{A+B+C}$
   B. $\overline{A}+\overline{B}+\overline{C}$
   C. $\overline{A}\overline{B}\overline{C}$
   D. $A+B+C$

Please turn over

13. A 2-input NOR gate with its two inputs shorted will act as a;
    A. AND Gate
    B. OR Gate
    C. NOT Gate
    D. XOR Gate

14. How many gates would be required to implement the Boolean expression XY + X(X+Z) +Y(X+Z) before simplification?
    A. 3
    B. 5
    C. 6
    D. 8

15. A group of flip-flops used for data storage is called;
    A. Registers
    B. JK Flip-flop
    C. Latch
    D. Counter

16. A logic circuit with an output $X = A\overline{B}C + A\overline{C}$ consists of;
    A. Two AND gates and one OR gate
    B. Two AND gates, one OR gate, and two inverters
    C. Two OR gates, one AND gate, and two inverters
    D. Two AND gates, one OR gate, and one inverter

17. One of the advantages of digital over analog representation is that;
    A. Data can be processed and transmitted more efficiently and reliably.
    B. Digital signals typically use less bandwidth.
    C. Data cannot become corrupted.
    D. Output is not subject to quantity errors from sampling

18. TTL IC's operating voltage is;
    A. 3V
    B. 5V
    C. 3.3V
    D. 5.5V

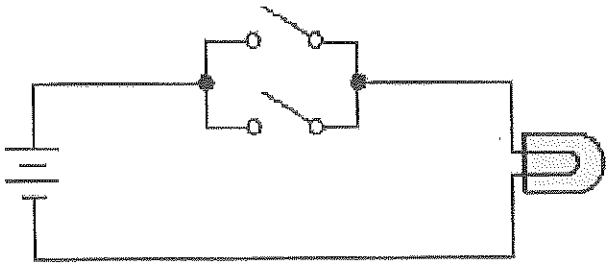
Please turn over

19. According to the Commutative Law of Addition,
    A. AB = BA
    B. A = A + A
    C. A + (B + C) = (A + B) + C
    D. A + B = B + A

20. A 4-variable Karnaugh map has;
    A. Eight cells
    B. Three cells
    C. Sixteen cells
    D. Four cells

Section B – True or False (10 marks)

1. The switch circuit diagram shown below is the equivalent logic function of an AND gate.



2. For three input variables, there are eight possible combinations of binary inputs to a gate.

3. The Boolean expression X = AB + CD represents two AND's ORed together.

4. According to the associative law of addition, A + (B + C) = (A + B) + C.

5. To determine the logic state of an output of a logic gate, the test instrument you will use is a Logic Probe.

6. A NOR gate output is LOW when all inputs are HIGH.

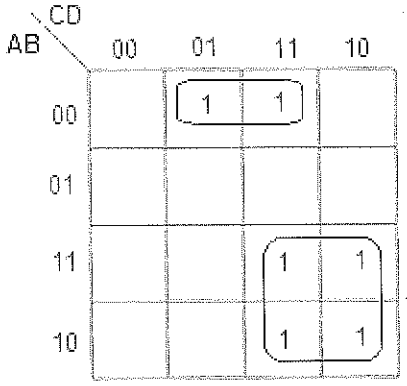
7. The binary number 1101010001101101 can be written in hexadecimal as $6A2F_{16}$.

Please turn over

8. A MOD 6 counter counts from 0 to 6.

9. If an S-R latch has a 1 on the S input and a 0 on the R input and then S input goes to 0, the latch will be SET.

10. The minimum SOP expression derived from the Karnaugh map below is $X = \overline{A}\overline{B}D + AD$.



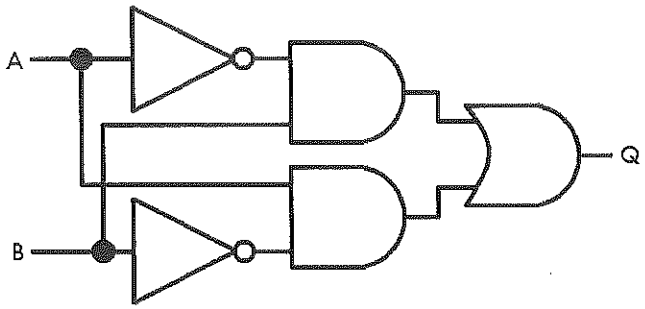
Section C – Short Answers [20 marks]

1. State DeMorgan's theorem. (2 mark)

2. Convert the Boolean expression, $\overline{\overline{(A+B)}+C}$ to SOP form. (2 marks)

3. Convert the binary number 11000110 to Gray code. (2 marks)

4. Draw the truth table to show the behavior of the following circuit.



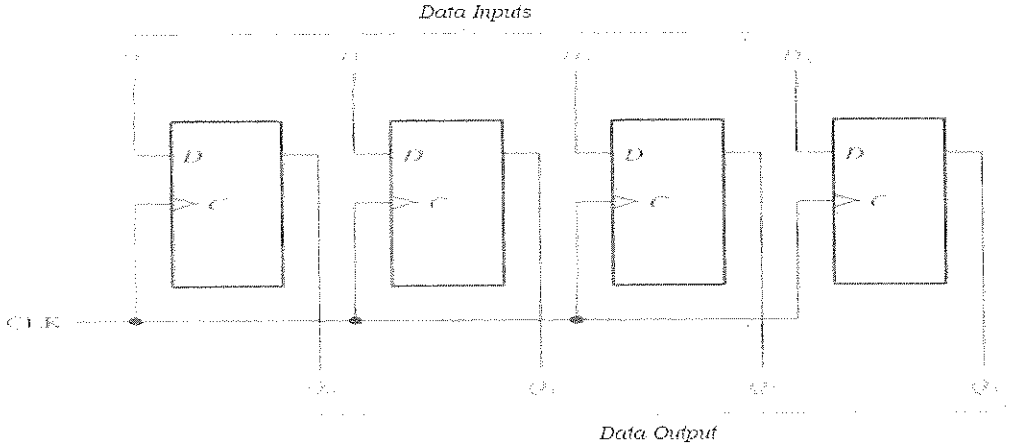
(2 marks)

Please turn over

5. Explain the following threshold voltage acronyms;
   A. V_{IL}
   B. V_{OH} (2 marks)

6. What is the difference between a CMOS and a TTL integrated circuit (IC) in terms of their operating voltages? (1 mark)

7. Identify the following circuit shown below;



(1 marks)

8. Develop a truth table for the POS expression; $(\overline{A}+\overline{B}+\overline{C})(A+B+C)(A+\overline{B}+C)$ (2 marks)

9. Use the Karnaugh map to find the minimum SOP form for the expression; $\overline{A}\overline{B}\overline{C}+A\overline{B}\overline{C}+\overline{A}B\overline{C}+AB\overline{C}$. (3 marks)

10. Implement the expression AB + CDE using NAND gates only. (3 marks)

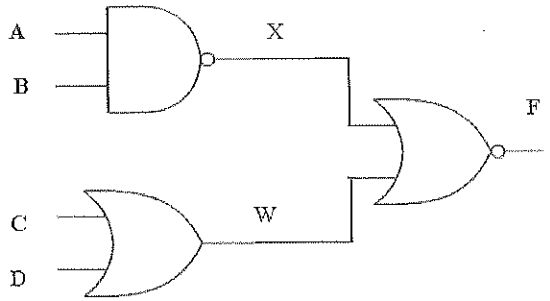
Section D – Calculations & Diagrams (40 marks)

Show your working clearly where necessary.

1. Convert the decimal number 163 to the following numbers using any of the conversion methods.
   A. Binary number (2 marks)
   B. Hexadecimal number (2 marks)
   C. Octal number (2 marks)

Please turn over

2. For the Logic Gates Circuit shown below;



A. Write down the Logic Expression at points W, X and F. (3 marks)
B. Determine the Truth Table for the circuit. (4 marks)

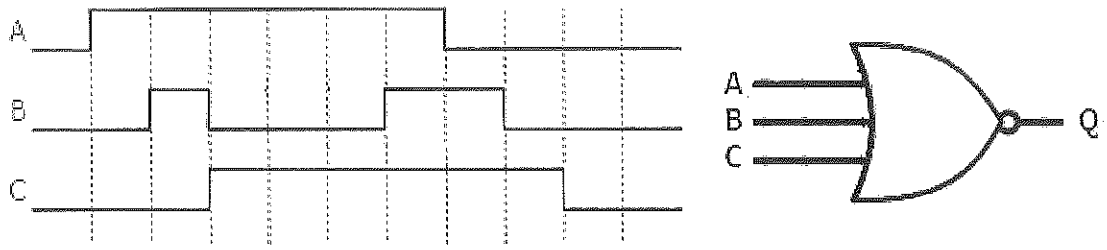
3. Convert the decimal number 75.5 to binary by using the sum-of-weights method. (2 marks)

4. Draw the logic diagram for the following Boolean expression given below:
A. Q = A (B+CD) (2 marks)
B. Q = AB + BCD + AC (2 marks)

5. What is the largest decimal number that can be represented in binary with six bits? (1 mark)

6. Design a mod-10 ripple counter using JK Flip-flops. Show all steps of your design clearly. (5 marks)

7. Determine the output waveform X for the input waveforms to a 3-input NOR gate as shown;



(4 marks)

Please turn over

8. Apply DeMorgan's theorem to each expression;
   A. $\overline{(A+B+C)D}$ (1 mark)
   B. $\overline{\overline{(A+B)}+\overline{C}}$ (2 marks)

9. Three switches A, B, C control a device. The device must operate if A is on and B is on but C is off, or if A is off B is on and C is on, or if A is on B is off and C is on. Under all other conditions the device must NOT operate. Take Q as the output.
   i. Draw the truth table (4 marks)
   ii. Write the Boolean expression (2 marks)

10. Using Boolean algebra techniques, simplify this expression;
    AB + A(B + C) + B(B + C) (2 marks)

Section E – Application Questions (10 marks)

1. A manufacturing plant uses two tanks to store a certain liquid chemical that is required in a manufacturing process. Each tank has a sensor that detects when the chemical level drops to 25% full. The sensors produce a 5V level when the tanks are more than one-quarter full. When the volume of chemical in a tank drops to one-quarter full, the sensor puts out a 0V level.
   It is required that a single green light-emitting diode (LED) on an indicator panel show when both tanks are more than one-quarter full. Show with an aid of a diagram, and briefly explain how a NAND gate can be used to implement this function. (5 marks)

2. The supervisor of the manufacturing process as described in above (question 1) has decided that he would prefer to have a red LED display come on when at least one of the tanks fall to the quarter-full level rather than have the green LED display indicate when both are above one-quarter. Show with an aid of a diagram, how this requirement can be implemented. (5 marks)

The End

----------GOOD LUCK----------