FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

TRADE DIPLOMA IN ELECTRONIC ENGINEERING

EEE475 – DIGITAL ELECTRONIC 1.

FINAL EXAMINATION – TRIMESTER 3 - 2015.

Duration: 3 hours

TIME: TBA **Date: TBA**

INSTRUCTIONS TO STUDENTS:

1. You are allowed 10 minutes **EXTRA** as reading time during which you are **NOT** to write.
2. Begin each answer on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each attached sheet.
4. Insert all written foolscap, graph paper, drawing paper, etc. in their correct sequence and secure well.
5. For all sheets of paper on which rough/draft work has been done, cross it through and attach to your answer scripts.
6. Show all workings where necessary
7. Diagrams and graphs can be drawn in pencil.
8. Non- programmable calculators are allowed.
9. Attempt all questions i.e. Sections A, B, C, D & E
10. **Check your work before you leave the room!!**

Section A: **(20 marks)**

Part 1 **MULTIPLE CHOICE**

Attempt all questions in this section by selecting and writing the correct alphabet beside the number. **(10 marks)**

1. What are the symbols used to represent digits in the binary number system

   (a) 0, 1
   (b) 0, 1, 2
   (c) 0 -8
   (d) 1, 2

2. In the NOR gate operation

   (a) Output is HIGH when all inputs are LOW
   (b) Output is Low when all inputs are HIGH
   (c) Output is HIGH when one input is HIGH
   (d) a & b

3. In a JK synchronous Flip Flop, if J = 1 and K = 0 then Q will

   (a) Change to 1 if it was on 0
   (b) Toggle
   (c) Remain on 0
   (d) not allowed

4. The output of an AND gate is LOW

   (a) all the time
   (b) when any input is LOW
   (c) when any input is HIGH
   (d) when all inputs are HIGH

5. Which of the following does not represents digital signal data?

   (a) ON and OFF states
   (b) 0 and 1
   (c) 1.5, 3.2, 4.8 and 5V
   (d) 0V and 5V

6. Using DeMorgans theorem, the expression $\overline{AB+DE}$ is equal to:

(a) $(\bar{A} + \overline{B})(\bar{D} + \bar{E})$
(b) $(\overline{AB})(\overline{DE})$
(c) (AB).(DE)
(d) Both a and b

7. A flip flop has

(a) one stable state
(b) no stable states
(c) two stable states
(d) none of the above

8. An Exclusive OR gate produces a "1" output when its two inputs are
(a) high
(b) Low
(c) Different
(d) Same

9. Which of the following will not produce an error code in BCD?

(a) 1011
(b) 0101
(c) 1100
(d) 1010

10. Which segments of a 7-segment display reads decimal 4?

(a) Segments f, g, b, c are lit
(b) Segments a, f, g, c, d are lit
(c) Segments b, c are lit
(d) Segments e, f are lit

Part 2 **Number System & Code**

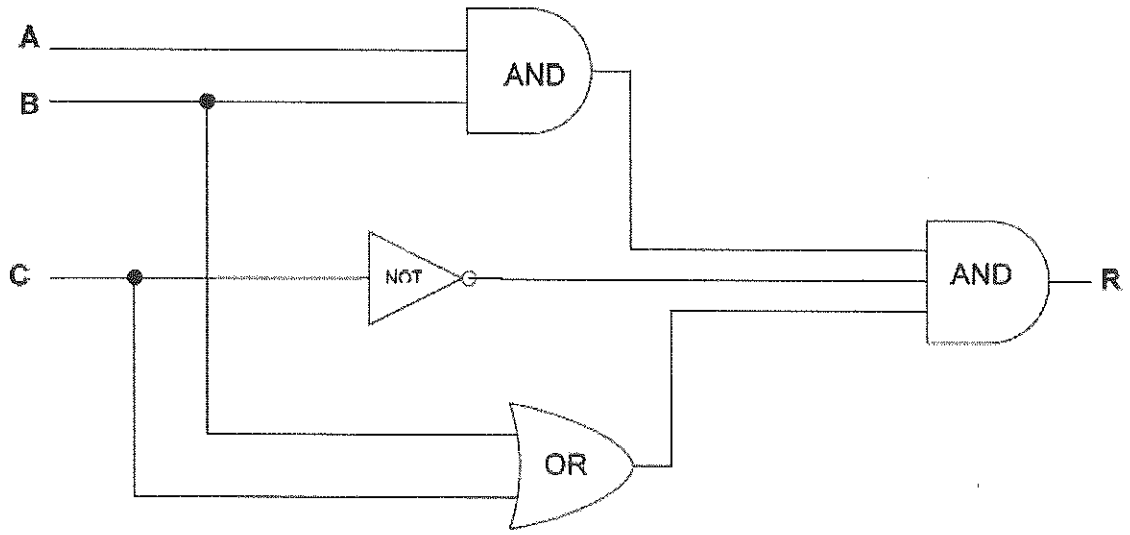
Question 1 **(10 marks)**

a) Convert fractional decimal number 6.75 to binary **(2 marks)**
b) Convert Octal number 724 to Decimal number. **(2 marks)**
c) Convert BCD number 101111000001 to Decimal number. **(2 marks)**
d) Convert Decimal number 489 to Excess-3 number **(2 marks)**
e) Convert Binary number 1011010111 to Octal number **(2 marks)**

Section B **Combinational Logic Circuits** **(20 marks)**

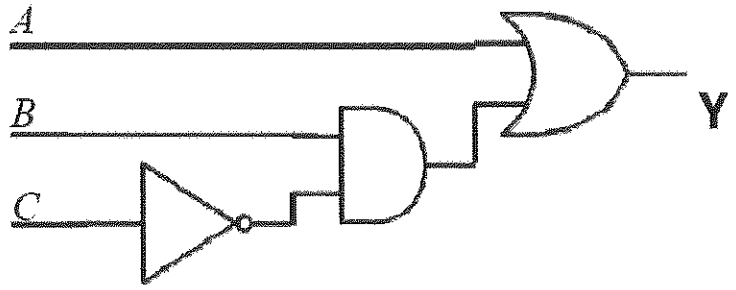
Question 1

Find the simplified Boolean expression for the circuit below; **(5 marks)**



Question 2

1. Complete the truth table for the combinational logic circuit below; **(4 marks)**



Question 3

Draw the combinational logic circuit for the Boolean expression $\overline{\overline{AB} + \overline{AC}}$ **(4 marks)**

Question 4

Derive the minterm Boolean expression from the truth table below. And draw the logic circuit diagram that represents this Boolean expression. **(7 marks)**

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Section C Karnaugh Map & Boolean Expression (20 marks)

Part 1

Question 1

Use the Karnaugh Map method to simplify the Boolean expression below; **(5 marks)**

$$Y = A\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C} + \overline{A}BC + ABC$$

Question 2

Use the Karnaugh Map method to simplify the Boolean expression below; **(5 marks)**

$$Y = \overline{A}\overline{B} + A\overline{C}$$

Question 3

Derive a simplified Boolean expression from the Karnaugh Map given below; **(4 marks)**

	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	1	0	1	0
$\overline{A}B$	0	0	1	0
AB	0	0	0	0
$A\overline{B}$	1	0	0	0

Part 2

Question 1

Simplify the Boolean expression $\overline{A}B + A\overline{B} + AB$ using Boolean algebra rules **(3 marks)**

Question 2

Prove the following Boolean identity $ABC + A\overline{B}C + AB\overline{C} = A(B+C)$ using the rules of Boolean algebra. **(3 marks)**

Section D Logic Families & Display Devices (20 marks)

Part 1

Question 1

Explain the TTL circuit operation when the state is LOW? **(5 marks)**

Question 2

Explain the TTL circuit operation when the state is HIGH? **(5 marks)**

Part 2

Question 1

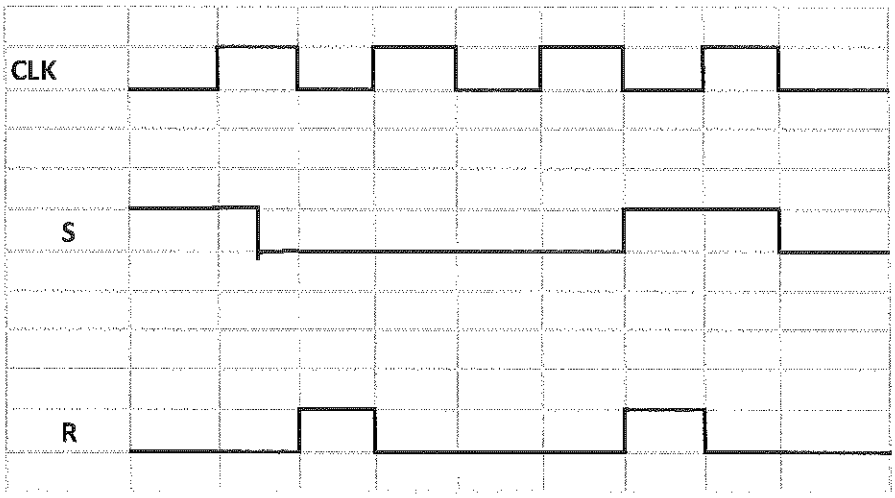
A customer wishes to purchase a 7-segment display (SSD) with a luminous intensity of 1.5. Draw the common cathode method to test the SSD brightness by testing the digit "2". **(10 marks)**

Section E Flip Flop & DAC/ADC Converters (20 marks)

Part 1

Question 1

a) Briefly explain with truth table and Q output timing diagram the operation of the SR nor gate flip flop (**5 marks**)

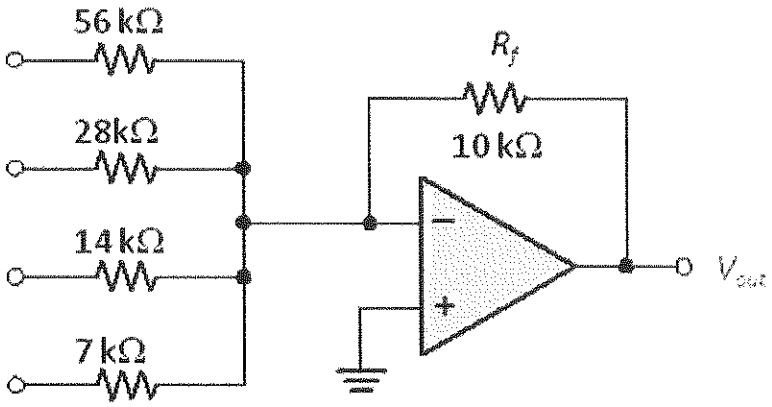


b) Briefly explain with truth table and Q output timing diagram the operation of the JK flip flop **(5 marks)**

Part 2

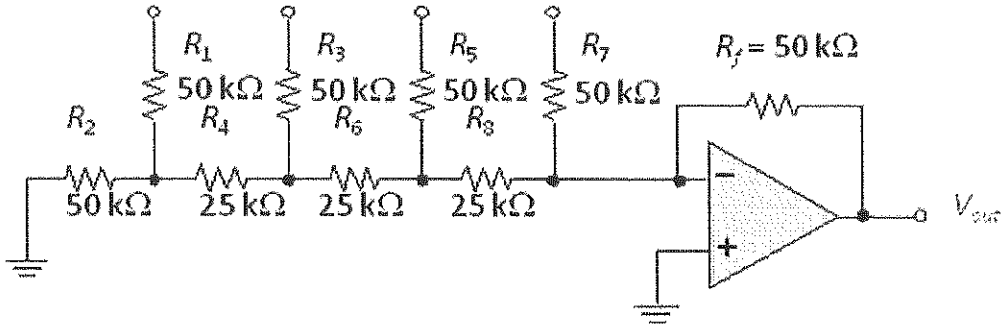
Question 1

A certain binary-weighted-input DAC has a binary input of 1010. If a HIGH = +5.0 V and a LOW = 0 V, what is V_{out}? **(5 marks)**



Question 2

A *R-2R* ladder DAC has a binary input of 1110. If a HIGH = +3.0 V and a LOW = 0 V, what is V_{out}? **(5 marks)**



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