FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

TRADE DIPLOMA IN ELECTRONIC ENGINEERING

EEE475 – DIGITAL ELECTRONIC 1.

FINAL EXAMINATION – TRIMESTER 1 - 2015.

Duration: 3 hours

TIME: TBA Date: TBA

INSTRUCTIONS TO STUDENTS:

1. You are allowed 10 minutes **EXTRA** as reading time during which you are **NOT** to write.
2. Begin each answer on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each attached sheet.
4. Insert all written foolscap, graph paper, drawing paper, etc. in their correct sequence and secure well.
5. For all sheets of paper on which rough/draft work has been done, cross it through and attach to your answer scripts.
6. Show all workings where necessary
7. Diagrams and graphs can be drawn in pencil.
8. Non- programmable calculators are allowed.
9. Attempt all questions i.e. Sections A, B, C, D & E
10. **Check your work before you leave the room!!**

Section A: (20 marks)

Part 1 **MULTIPLE CHOICE**

***Attempt all questions in this section by selecting and writing the correct alphabet beside the number*.** **(10 marks)**

1. In a binary system, the right-most digit is the

   (a) High significant bit
   (b) Least significant bit
   (c) Most significant bit
   (d) Standard significant bit.

2. In the NOR gate operation

   (a) Output is HIGH when all inputs are LOW
   (b) Output is Low when all inputs are HIGH
   (c) Output is HIGH when one input is HIGH
   (d) a & b

3. In a JK synchronous Flip Flop, if J = 1 and K = 0 then Q will

   (a) Change to 1 if it was on 0
   (b) Toggle
   (c) Remain on 0
   (d) not allowed

4. What input combination will produce a LOW at the output of a 3-input OR gate?

   (a) When all inputs are LOW
   (b) When any one input is HIGH
   (c) When two inputs are logic 1
   (d) When any one input is LOW

5. Which of the following does not represents digital signal data?

   (a) ON and OFF states
   (b) 0 and 1
   (c) 1.5, 3.2, 4.8 and 5V
   (d) 0V and 5V

6. Using DeMorgans theorem, the expression $\overline{AB + DE}$ is equal to:

(a) $(\bar{A} + \bar{B} + (\overline{D} + \bar{E})$
(b) $(\overline{\mathrm{AB}})(\overline{\mathrm{DE}})$
(c) (AB).(DE)
(d) Both c and d

7. Which of the following logical operation is represented by the + sign in Boolean algebra?

(a) Inversion
(b) NOR
(c) AND
(d) OR

8. An Exclusive OR gate produces a "1" output when its two inputs are
(a) high
(b) Low
(c) Different
(d) Same

9. Which of the following will not produce an error code in BCD?

(a) 1011
(b) 0101
(c) 1100
(d) 1010

10. Which segments of a 7-segment display reads decimal 4?

(a) Segments f, g, b, c are lit
(b) Segments a, f, g, c, d are lit
(c) Segments b, c are lit
(d) Segments e, f are lit

Part 2 **Number System & Code**

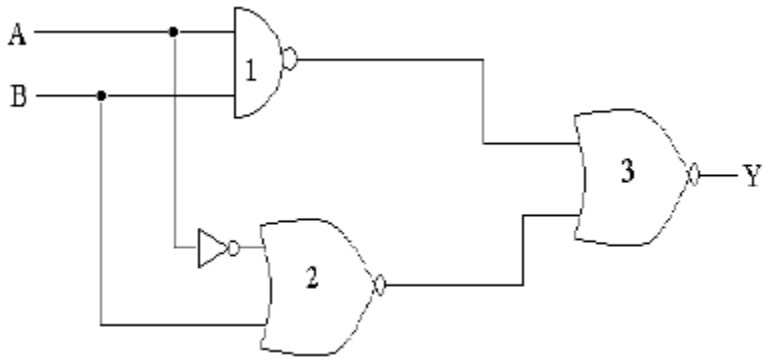
Question 1 **(10 marks)**

a) Convert Binary number 010101 to Gray code. **(2 marks)**
b) Convert Octal number 724 to Decimal number. **(2 marks)**
c) Convert BCD number 011111000001 to Decimal number. **(2 marks)**
d) Convert Decimal number 489 to Excess-3 number **(2 marks)**
e) Convert Binary number 1011010111 to Octal number **(2 marks)**

Section B Combinational Logic Circuits (20 marks)

Question 1

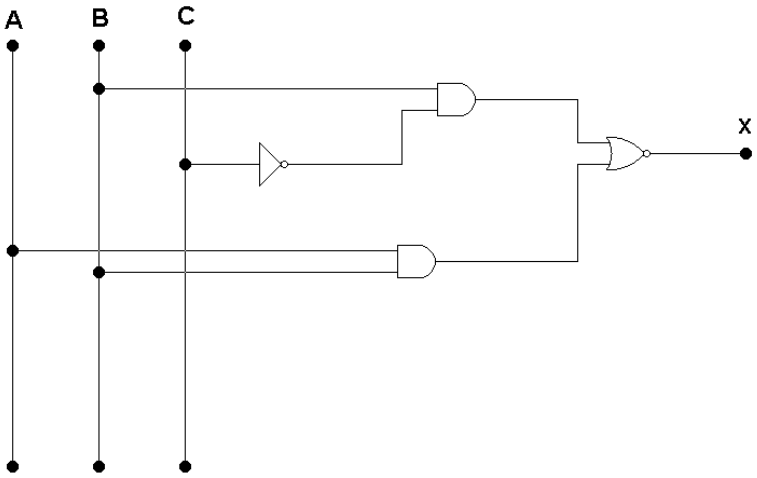
Find the simplified Boolean expression for the circuit below; **(5 marks)**



Logic Gate 1 = NAND gate
Logic Gate 2 = NOR gate
Logic Gate 3 = NOR gate

Question 2

1. Complete the truth table for the combinational logic circuit below; **(4 marks)**



Question 3

Draw the combinational logic circuit for the Boolean expression $Y = \overline{\overline{A+B} \cdot \overline{C}}$ **(4 marks)**

Question 4

Derive the Boolean expression from the truth table below. And draw the logic circuit diagram that represents this Boolean expression. **(7 marks)**

A	B	X
0	0	1
0	1	1
1	0	0
1	1	0

Section C Karnaugh Map & Boolean Expression (20 marks)

Part 1

Question 1

Use the Karnaugh Map method to simplify the Boolean expression below; **(5 marks)**

$$A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} = Y$$

Question 2

Derive a truth table from the given Boolean expression; **(5 marks)**

$$\overline{A} \cdot \overline{B} + A \cdot B \cdot C = Y$$

Question 3

Derive a simplified Boolean expression from the Karnaugh Map given below; **(4 marks)**

	C'D'	C'D	CD	CD'
A'B'	0	0	1	1
A'B	0	0	0	0
AB	1	0	0	0
AB'	1	0	0	0

Part 2

Question 1

Simplify the Boolean expression $\overline{A}.B + A.\overline{B} + A.B$ to its simplest form. **(3 marks)**

Question 2

Prove the following Boolean identity ABC + AB'C + ABC' = A(B+C) using the laws of Boolean algebra. **(3 marks)**

Section D Logic Families & Display Devices (20 marks)

Part 1

Question 1

Explain the TTL circuit operation when the state is LOW? **(5 marks)**

Question 2

Explain the TTL circuit operation when the state is HIGH? **(5 marks)**

Part 2

Question 1

A customer wishes to purchase a 7-segment display (SSD) with a luminous intensity of 1.5. Draw the common cathode method to test the SSD brightness by testing the digit "2". **(10 marks)**

Section E Flip Flop & DAC/ADC Converters (20 marks)

Part 1

Question 1

a) Give one difference between the Flip flops and combinational logic circuits **(1 mark)**

b) From lab experience what was the Q and Q' output when SR were both "1" **(2 marks)**

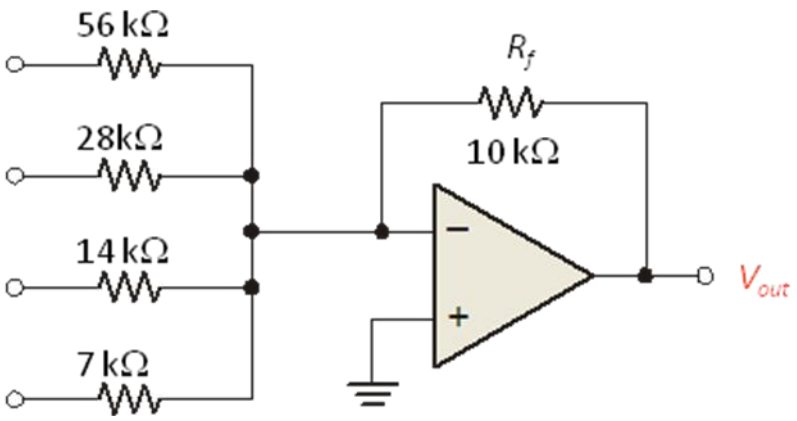
c) What is one advantage of the JK flip flop over the SR flip flop **(2 marks)**

d) Briefly explain with truth table the operation of the JK flip flop **(5 marks)**

Part 2

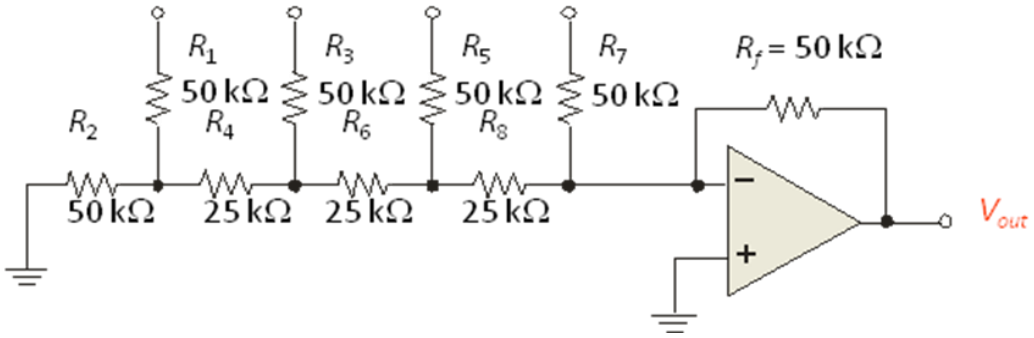
Question 1

A certain binary-weighted-input DAC has a binary input of 1010. If a HIGH = +5.0 V and a LOW = 0 V, what is V_{out}? **(5 marks)**



Question 2

A *R-2R* ladder DAC has a binary input of 1110. If a HIGH = +3.0 V and a LOW = 0 V, what is V_{out}? **(5 marks)**



----------THE END----------