FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE & TECHNOLOGY (CEST)

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

TRADE DIPLOMA IN ELECTRICAL ENGINEERING

(TELECOM AND NETWORKING) – STAGE 2

EEE435- ANALOGUE ELECTRONICS 2A

FINAL EXAMINATION – SEMSTER 2, 2015

EXAM DURATION: 2HRS

INSTRUCTIONS TO STUDENTS

1. You are allowed 10 minutes Extra reading time during which you are NOT to write.

2. Begin each answer on a fresh page and use both sides of the sheet.

3. Write your candidate-number at the top of each attached sheet

4. Insert all written foolscaps, graph paper, drawing paper, etc. in their correct sequence and secure with string

5. For all sheets of paper on which rough/draft work has been done, cross it through and you MUST ATTACH to your answer scripts.

6. Write clearly the number(s) of the question(s) attempted on the top of each sheet.

7. ANSWER ALL QUESTIONS.

8. Show all workings where necessary.

9. Do not use programmable calculators.

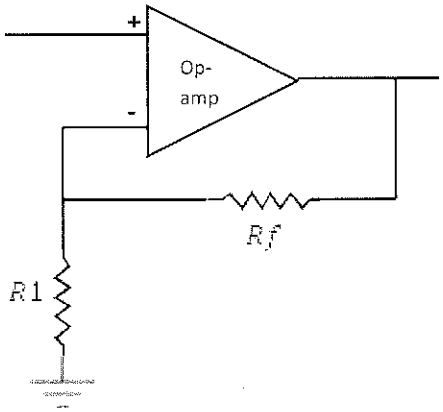
*10. **ALWAYS CHECK YOUR WORK BEFORE YOU LEAVE THE ROOM!***

Section A **Multiple Choice** [20 Marks]

Circle correct letter (A, B, C or D) against each of numbers 1 through 30.
Remove and attach to your Answer Booklet.

1. **How many layers does a transistor have?**
   A. 1
   B. 2
   C. 4
   D. 3

2. **Calculate the overall voltage gain of the circuit if $R1 = 200\Omega$ and $Rf = 20k\Omega$**



   A. -100
   B. -110
   C. 111
   D. 101

3. **What is the slew rate of an op-amp if the output voltages change from 4V to 6V in 0.5ms?**

   A. 4 V/ms
   B. 3 V/ms
   C. 2 V/ms
   D. 5 V/ms

4. **If Av(d) = 250 and Acm = 0.025, the CMRR is**

   A. 625
   B. 10,000

C. 80dB
D. Answer B and C

5. **Which of the following pin numbers represent the output terminal of LM741 operational amplifier?**

A. 2
B. 3
C. 4
D. 6

6. **In PNP transistor, the P-Region are**

A. Base and emitter
B. Base and collector
C. Emitter and collector
D. Only base

7. **If I_c is 100 times larger than I_B, then β is**

A. 0.02
B. 100
C. 50
D. 500

8. What is the output voltage of the fixed regulator type?
7924

a) -24 V
b) +12 V
c) +79 V
d) -92 V

9. **BJT is a _____ controlled device. The JFET is a _____ controlled device**

A. Voltage, voltage
B. Voltage, Current
C. Current, Voltage
D. Current, Current

10. **A JFET always operates with**

A. The gate-to-source *pn* junction reversed-biased
B. The gate-to-source *pn* junction forward-biased
C. The drain connected to ground
D. The gate connected to source

11. **If the supply frequency of a single phase is 50 hertz, the ripple frequency of a half -wave rectifier is:**

a) 100 Hz.
b) 12.5 Hz.
c) 25 Hz.
d) 50 Hz.

12. **When operated in the active region, the transistor acts like**

A. A switch
B. An amplifier
C. A variable capacitor
D. A variable resistor

13. **One disadvantage of linear power supply over Switched mode power supply is**
A. Operate at low frequency
B. Operate at low efficiency
C. Operate at high efficiency
D. Operate at high voltages only.

14. **The JFET is**
A. a unipolar device
B. a voltage controlled device
C. a current controlled device
D. Answers (A) and (B)

15. **The perfect circuit used for buffering the input of the inverting amplifier called:**
A. audio amplifier
B. voltage follower
C. non – inverting amplifier
D. summing amplifier

16. **The formula for closed loop gain of a non-inverting operational amplifier is:**
    A. $A_{CL} = -R_1/R_F$
    B. $A_{CL} = -R_F/R_1$
    C. $A_{CL} = 1 + R_F/R_1$
    D. $A_{CL} = -R_F/_{R1} + 1$

17. **If β_{DC} is 100 and I_B is 400 µA, then the I_C is**
    A. 40mA
    B. 40,000mA
    C. 40,000µA
    D. Both A and C

18 **For a certain JFET, I_{GSS} = 10nA at V_{GS} = 10V. The input resistance is**
    A) 100MΩ
    B) 1MΩ
    C) 1000MΩ
    D) 1000mΩ

19. **For a properly biased PNP transistor, let I_C=10mA and I_E=10.2mA. What is the level of I_B?**
    A. 0.2A
    B. 200mA
    C. 200µA
    D. 20.2mA

20. **What is the ratio of I_D/I_{DSS} for V_{GS} =0.5V_P?**
    A) 0.25
    B) 0.5
    C) 1
    D) 0

SECTION B [10 Marks]

Choose either **True or False** for the following question

1. A diode conducts current when forward biased and blocks current when reversed biased.
2. The forward biased barrier potential is 0.3V for silicon diode and 0.7V for Germanium diode.
3. The PIV for each diode in a center-tapped full wave rectifier is twice the output voltage.
4. The biased polarity for NPN and PNP is the same.
5. Testing the transistor to determine if it is good or bad can be done by physically checking the terminal leads.
6. The zener diode can be used to provide a reference voltage.
7. B_{dc} is usually designated as h_{FE} on the data sheets.
8. There are three junction on the bipolar junction transistor
9. When the BJT is in saturation, it act as an amplifier.
10. A full wave centre – tap rectifier uses 2 diodes.

SECTION C (20 Marks)

1. Sketch P-N Junction diode in the **Forward** bias and **Reverse bias** condition when a source supply voltage is connected to it. **(2 marks)**

2. Explain in your own words what do you understand by the following terms in Operational Amplifier circuits.

   i) Common Mode Input.
   ii) Open Loop Gain.
   iii) Common Mode Rejection Ratio (CMRR) **(6 marks)**

3. With the use of suitable sketches clearly describe the operation of a **Full-Wave Center – tap Rectifier circuit.**

   (Marks: Cct-2, Waveforms-2, Operation-2) **(6 marks)**

4. Use the **BJT Data Sheet** provided to answer the questions asked.

TYPE	CASE	POL MAT	V_{CE}	V_{CB}	$I_{C\ mA}$	V_{CES} @$I_{C\ mA}$	H_{fe} @ $I_{C\ mA}$	P(TOT) mW	USE	EQUIVALENT
BD140	TO-126	PS	80	100	1.5A	0.5@500	40@250	8W	G.P. o/p	40410
BC107	TO-18	NS	45	50	100	0.25@10	110@450	300	G.P.S.S. amp	BC207, BC147, BC182
BC559	TO-92 VAR 1	PS	30	30	100	0.65@100	125@800	500	G.P.S.S. amp	BC159
2N3055	TO-3	NS	60	70	15 A	1.1@4A	20@70 4A	115W	G.P. power	BDY 20
TIP 3055	TOP-3	NS	70	100	15 A	1.1@4A	20@ 4A	90W	Power output	MJE 3055

i. Current gain of BC147 and what current can this transistor operate from? **(1 mark)**
ii. Material used in all transistors? **(1 mark)**
iii. Abbreviation of G.P.S.S. from the table. **(1 mark)**
iv. Power dissipation of BC559? **(1 mark)**
v. Package of 2N3055? **(1 mark)**
vi. Polarity of the BC107 transistor? **(1 mark)**

SECTION D [25 Marks]

1. Draw the Physical and Symbolic Representation of the two types of Bipolar Junction Transistor. Label the terminals. **(4 marks)**

2. For the block diagram of the switched mode power supply given below in **Figure 2 - D**, explain the functions of the following blocks:
   i) Switching Element **(2 marks)**
   ii) High frequency Oscillator **(2 marks)**
   iii) Pulse width modulator **(2 marks)**

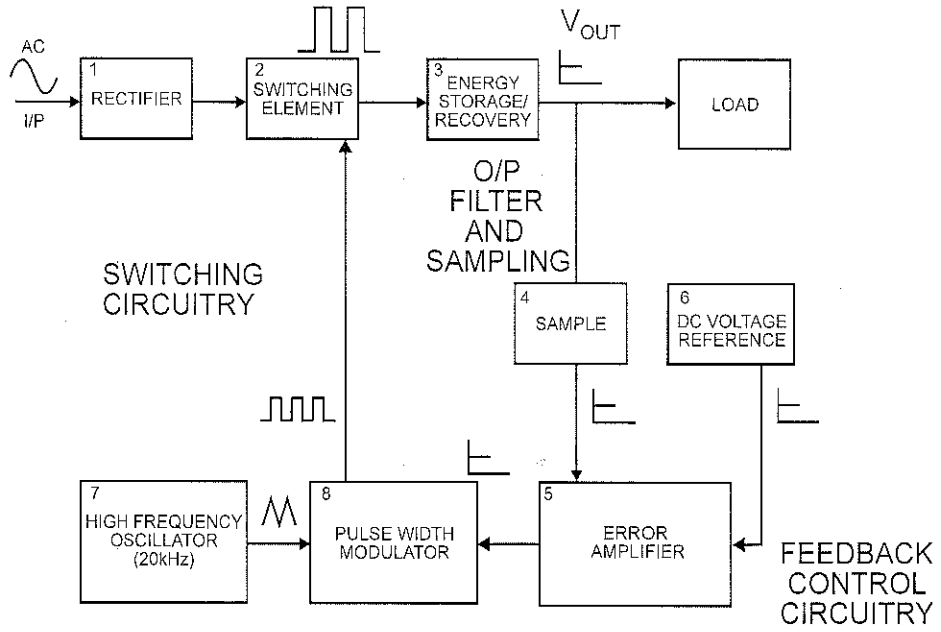


Figure 2 - D

3. **Fig 2-c** below shows a circuit diagram of an Op–Amp circuit.
   a. Identify the circuit below. **(1 mark)**
   b. Calculate the **output Voltage (V_o)**. **(3 marks)**

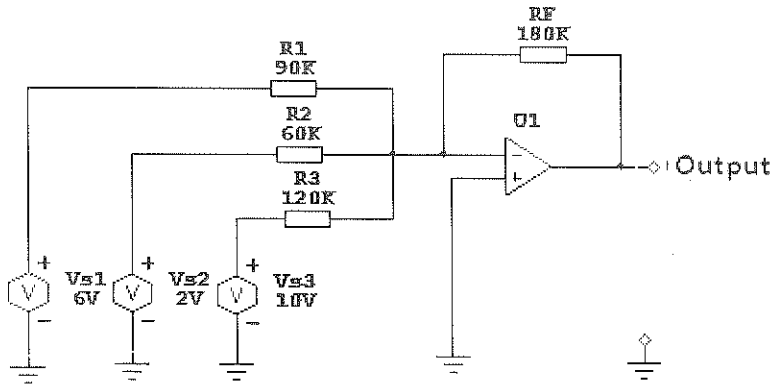


Fig - 2C

4. **Fig 2-E** shows a circuit of a **Junction Field Effect Transistor** (JFET). It shows biased voltages applied to an N – Channel device.

   Clearly explain the JFET Operation from the circuit below.

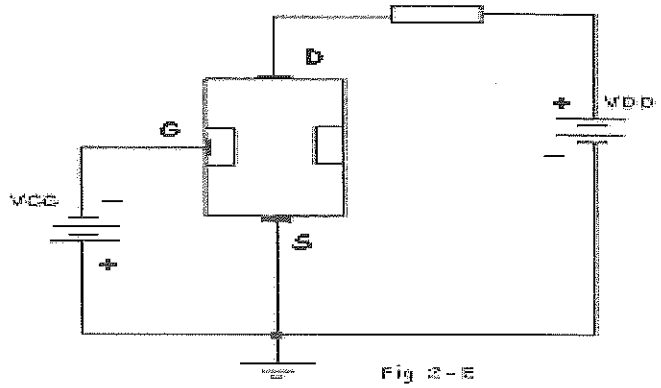
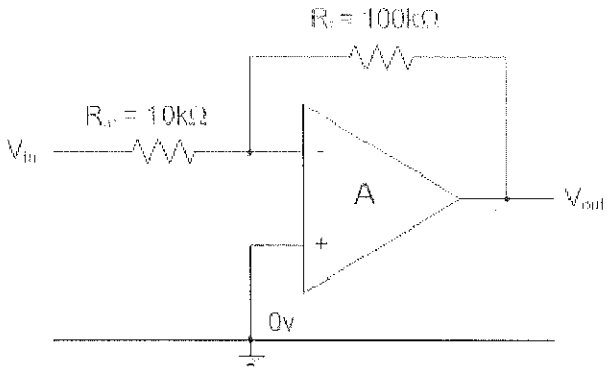


Fig 2-E

(6 marks)

5. Find the closed loop gain of the following inverting amplifier circuit.



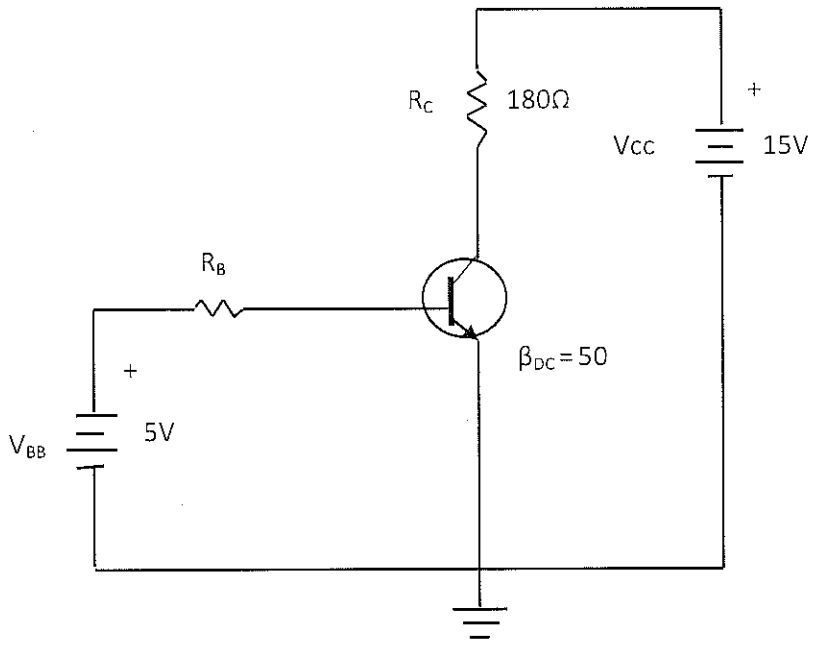
(3 marks)

6. Sketch the following circuit symbol:

   a. P Channel JFET (1 mark)
   b. N Channel E - MOSFET (1 mark)

SECTION D (25 Marks)

1. A silicon transistor having β_{DC} = 50 is shown below.



Determine the following:

i. V_{BE} **(1 mark)**
ii. I_B **(2 marks)**
iii. I_C **(1 mark)**
iv. I_E **(1 mark)**
v. V_{CE} **(2 marks)**
vi. V_{CB} **(1 mark)**

2.

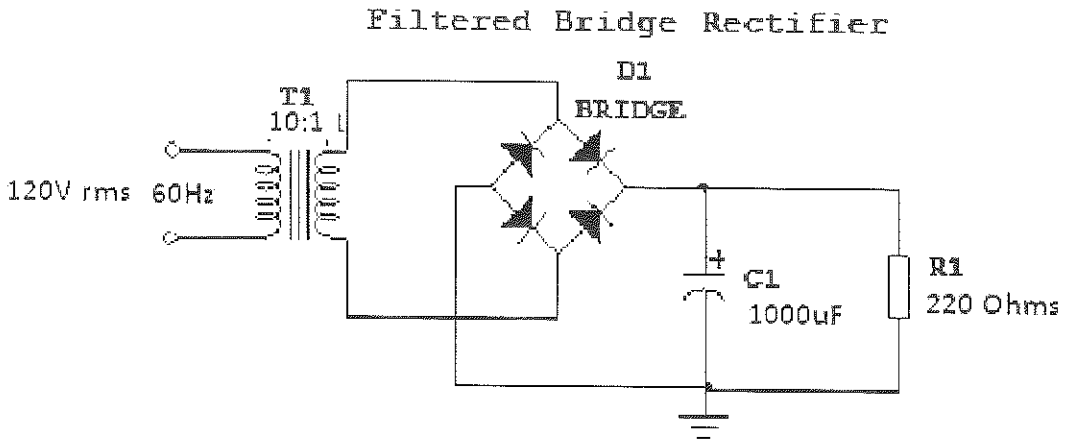
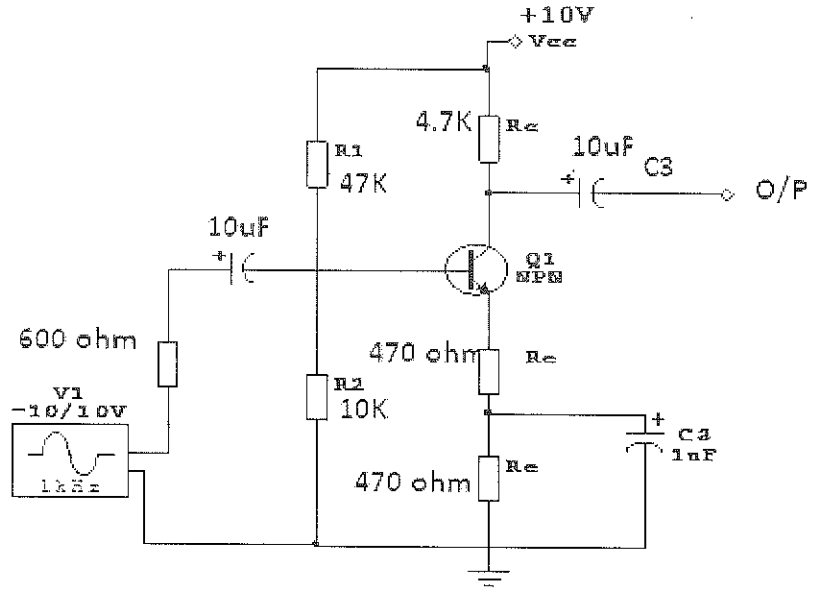


Figure 2-c

Refer to Figure 2-c to answer the following questions:
Calculate:

a. The peak primary voltage. (1 mark)
b. The peak secondary voltage (1 mark)
c. The unfiltered peak full wave rectified voltage (1 mark)
d. The peak –to- peak ripple voltage at the output (2 marks)
e. The dc output voltage (2 marks)

3.



$B_{DC} = 150$

Figure 3-C

Refer to **Figure 3-C** to answer question below to answer the dc bias values of Common Emitter Amplifier circuit.

Calculate:

a. R_{TH} (2 marks)
b. V_{TH} (2 marks)
c. I_E (2 marks)
d. I_C (1 mark)
e. V_E (1 mark)
f. V_B (1 mark)
g. V_C (1 mark)

THE END

FIJI NATIONAL UNIVERSITY

Candidate No: .....

Section A **Multiple-Choice Matrix** **[20 marks]**

Circle the correct letter (A, B, C or D) against each of numbers 1 through 30.

Remove and attach to your Answer Booklet.z

1	A	B	C	D
2	A	B	C	D
3	A	B	C	D
4	A	B	C	D
5	A	B	C	D
6	A	B	C	D
7	A	B	C	D
8	A	B	C	D
9	A	B	C	D
10	A	B	C	D
11	A	B	C	D
12	A	B	C	D
13	A	B	C	D
14	A	B	C	D
15	A	B	C	D
16	A	B	C	D
17	A	B	C	D
18	A	B	C	D
19	A	B	C	D
20	A	B	C	D