FIJI NATIONAL UNIVERSITY

College of Engineering, Science and Technology (CEST)

# EEE743 CONTROL SYSTEMS

## Final Examination

**Tuesday 17th June, 2014 1400 - 1710 hours Venue: B314**

### INSTRUCTIONS TO CANDIDATES

1. Candidates are reminded that they should have no books, notes, paper or other material in their possession unless their use is specifically permitted by "Instructions to Candidates" set out below.
2. Reading time is of 10 minutes duration.
3. Examination time is of 3 hours duration.
4. This paper consists of 8 questions printed on 8 pages.
5. Attempt all 7 questions. Each question may carry a different mark.
6. A set of Laplace Transforms Table is attached.
7. The datasheet for the 74LS153 Multiplexer is on page 3.
8. Write your candidate number at the top of each attached sheet.
9. Start each question on a new page.
10. Non-Programmable Calculators may be used.
11. Mobile phones are not allowed inside the examination venue.

**QUESTION 1: FIRST ORDER *RC* & *RL* NETWORKS [TOTAL: 14 MARKS]**

(a) The 1st Order *RC* circuit in Figure 1 has zero initial conditions. The switch S1 is closed at time $t = 0$.

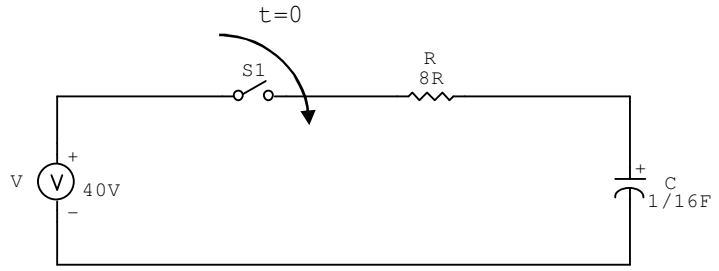



**Figure 1: 1st Order *RC* network**

(i) Determine the solution, $q(t)$, by applying Kirchoff's Voltage Law (KVL) and using conventional Calculus. Identify the Steady State and the Transient State. [**5 marks**]

(ii) Resolve for $q(t)$ using Laplace Transforms. [**4 marks**]

(iii) Derive the expression for the instantaneous current, $i(t)$. [**2 marks**]

(iv) Given the step response of a 1st Order System, $C(s) = \frac{5}{s(s+2)}$, use the method of Poles & Zeros to determine time-domain response. [**3 marks**]

**QUESTION 2: SECOND ORDER SYSTEMS & SERIES RLC NETWORK [TOTAL: 15 MARKS]**

(a) Given an Underdamped system, find the following if the Transfer Function is

$$G(s) = \frac{36}{s^2 + 9s + 36}$$

(i) Peak time ($T_p$) **[4 marks]**

(ii) Percentage Overshoot **[3 marks]**

(iii) Settling time ($T_s$) **[2 marks]**

(b) Refer to the Series *RLC* circuit shown in Figure 2. The output is taken across the capacitor, *C*. Use Laplace Transforms to derive the solution of q(t). Assume zero initial conditions. **[6 marks]**

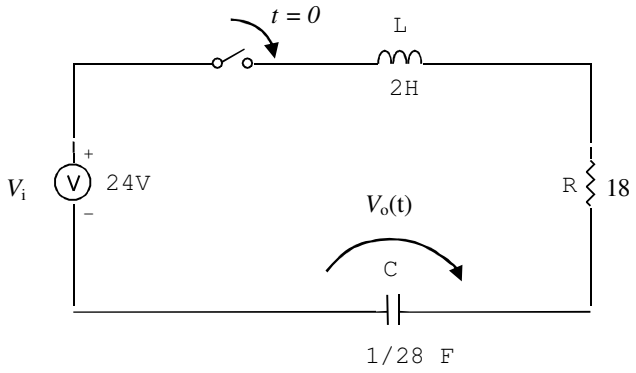



**Figure 2: Series *RLC* circuit**

**QUESTION 3 : ROOT LOCUS [TOTAL: 12 MARKS]**

Consider the system shown in Figure 3.

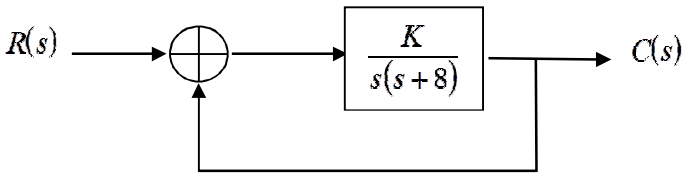



**Figure 3: A 2nd Order System**

(a) Derive the Characteristic Equation in quadratic form. **[3 marks]**

(b) Sketch the Root Locus. [Hint: Obtain roots for k = 0, 4, 8, 12, 16, 20] **[5 marks]**

(c) Find the value(s) of k that make the system overdamped, but will keep the system stable. **[4 marks]**

**QUESTION 4: LAPLACE TRANSFORMS; UNIT STEP FUNCTION [TOTAL: 12 MARKS]**

(a) Determine the s-domain equivalents of the following functions using the given table of Laplace Transform.

(i) $f(t) = -7\cos 4t + 3e^{2t} - 5t^3$ **[2 marks]**

(ii) $f(t) = 2e^{3t}\sin 5t$ **[2 marks]**

(iii) $f(t) = \begin{Bmatrix} (t-5)^3, & t > 5 \\ 0, & t < 5 \end{Bmatrix} = u(t-5)(t-5)^3$ **[2 marks]**

(b) Sketch the functions,

(i) $f(t) = 4[u(t) - u(t-3)]$ **[2 marks]**

(ii) $f(t) = u\left(t - \frac{\pi}{2}\right)\cos t, \quad 0 \le t \le 2\pi$ **[2marks]**

(iii) $f(t) = u(t).t^2, \quad f(t+2) = f(t); \quad 0 \le t \le 6$ **[2marks]**

**QUESTION 5 : SIGNAL CONDITIONING [TOTAL: 12 MARKS]**

(a) Consider a 4-bit DAC using an op-amp summing amplifier with binary-weighted resistors as shown in Figure 4.

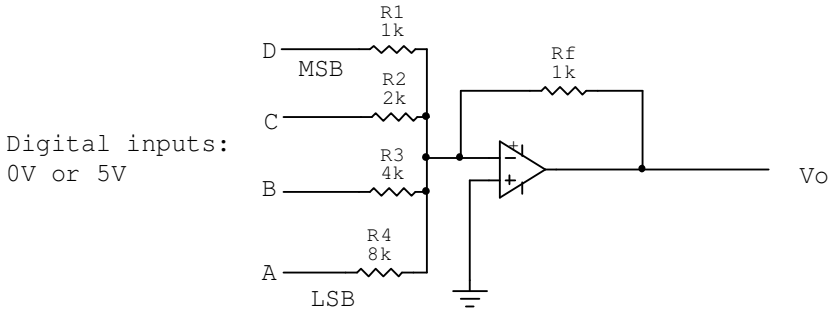



Figure 4: 4-bit DAC

**[5 marks]**

Determine the step size (resolution) and find the output voltages for all the combinations of the input code, from DCBA = 0000 to 1111. Tabulate your results as shown in Table 1:

| D | C | B | A | | $V_{out}$ (v) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | |
| 0 | 0 | 0 | 1 | | |
| 0 | 0 | 1 | 0 | | |
| 0 | 0 | 1 | 1 | | |
| 0 | 1 | 0 | 0 | | |
| 0 | 1 | 0 | 1 | | |
| 0 | 1 | 1 | 0 | | |
| 0 | 1 | 1 | 1 | | |
| 1 | 0 | 0 | 0 | | |
| 1 | 0 | 0 | 1 | | |
| 1 | 0 | 1 | 0 | | |
| 1 | 0 | 1 | 1 | | |
| 1 | 1 | 0 | 0 | | |
| 1 | 1 | 0 | 1 | | |
| 1 | 1 | 1 | 0 | | |
| 1 | 1 | 1 | 1 | | |

Table 1: DAC Table

(b) Describe concisely how the ADC illustrated in Figure 5 operates. **[5 marks]**

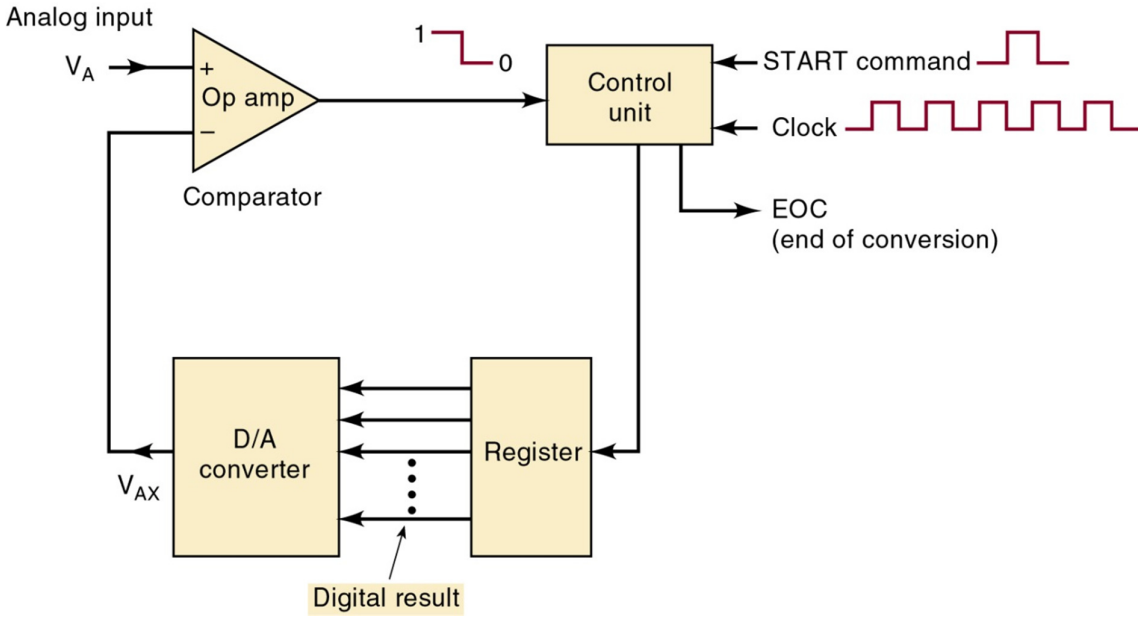



Figure 5: ADC

(c) Refer to Table 1, showing the Function Table for the Full Adder (Binary Adder). Design a circuit using the 74LS153 Multiplexer to implement the Sum (S) and the Carry Out ($C_{out}$). Both outputs S and $C_{out}$ are to be present at any time. (Note: Datasheet for 74LS153 is provided).

Table 2: Binary Adder

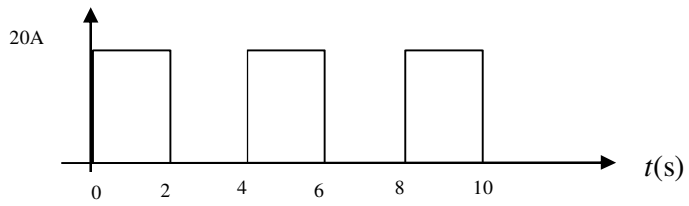
| A | B | K | S | $C_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**[5 marks]**

**QUESTION 6 [FOURIER SERIES, NOISE, BANDWIDTH] [TOTAL: 20 MARKS]**

(a) Analyse the current pulse train shown.

(i) Determine the amplitude and frequency of the fundamental and harmonic content through the first seven harmonics. The pulse train represents the function $i(t)$ $\begin{cases} 20, & 0 \le t < 2 \\ 0, & 2 \le t < 4 \end{cases}$; $i(t+4) = i(t)$




**[5 marks]**

(ii) Predict the amplitude and the frequency for the term when n = 13. **[2 marks]**

(b) A communication equipment with a gain of 120 and a bandwidth of 2 MHz has an input resistance of 8 kΩ. It is operating at a temperature of 27 °C and receives an input audio signal of 6 $uV_{rms}$. Given Boltzmann's constant is 1.38 x $10^{-23}$ J/K, calculate the following

(i) White [Johnson] Noise Power **[2 marks]**

(ii) RMS input noise level **[2 marks]**

(iii) Audio output level **[2 marks]**

(iv) RMS output noise level **[2 marks]**

(b) The bandwidth, *B*, of the PSTN is 4 kHz.

(i) Assume a noiseless environment and use the Nyquist (Hartley) equation, $C = 2B\log_2 M$ , to resolve for the Maximum Data Transfer Rate (Capacity). There are 16 signalling levels. **[2 marks]**

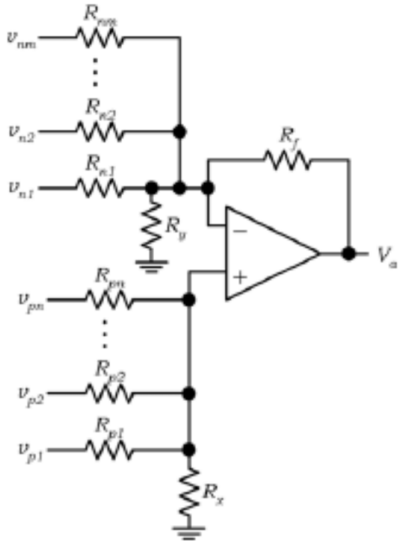
(ii) If the S/N ratio is 50 dB, determine the maximum information rate, *C*, predicted by Shannon's law, $C = B\log_2\left(1+\frac{S}{N}\right)$. **[3 marks]**

**QUESTION 7 OPERATIONAL AMPLIFIERS – ANALOGUE COMPUTERS [TOTAL: 10 MARKS]**

Design an Analogue Computer using Operational amplifiers to solve the second order differential equation, $v'' = 5v' - v + 4\cos 10t$. Use integrators whose time constant *RC* = 1. Assume the initial conditions v'(0) = 0 and v"(0) = 2 V. Provide a block diagrammatic representation of the circuit first. State any assumptions you make. Do note the General Add-Subtract circuit shown in

Figure **6**, and the parameters that need to be evaluated.

**[10 marks]**




$$V_o = \sum_{i=1}^{n} A_i v_{pi} - \sum_{i=1}^{m} B_i v_{ni}$$

where, $A_i = \frac{R_f}{R_{pi}}, B_i = \frac{R_f}{R_{ni}}$

Let $A = \sum A_i, B = \sum B_i$

Let $C = A - B - 1$

If

$$\begin{cases} C \geq 0 & R_x = \infty \quad R_y = \frac{R_f}{C} \\ C < 0 & R_x = -\frac{R_f}{C} \quad R_y = \infty \end{cases}$$

**Figure 6: General Add-Subtract circuit**

**QUESTION 8: PARALLEL RLC NETWORK** **[TOTAL: 12 MARKS]**

(a) Analyse the Parallel RLC network shown.

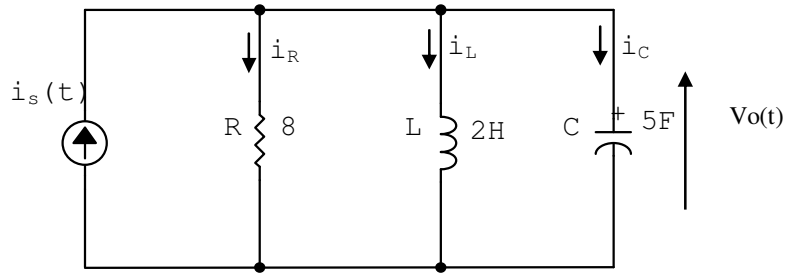



**Figure 7: Parallel *RLC* network**

(i) Analyse the network and derive the mathematical model in the s-domain. Assume zero initial conditions. **[4 marks]**

(ii) Construct the block diagram of the network, then reduce it to its simplest Closed-loop form using the block reduction technique. **[4 marks]**

(iii) Find the Closed-loop Transfer Function. Represent this via a block diagram. **[4 marks]**

**[THE END]**