FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

BACHELOR OF ENGINEERING

EEE627 – LOGIC DESIGN 1

SEMESTER 1, 2014

DAY/DATE: As timetabled DURATION : Three hours

ROOM: As timetabled

INSTRUCTION TO STUDENTS

1. You are allowed 10 minutes extra reading time during which you are **NOT** to write.
2. Answer ALL questions in Section A and FOUR questions in Section B
3. **Begin the answer to each Question** on a fresh page and use both sides of the sheet.
4. Write clearly the number of the question attempted on the top of each sheet
5. Write your candidate number at the top of each sheet & attach them.
6. Insert all written foolscaps, graph paper etc. in their correct sequence and secure with a string.
7. All sheets of paper on which rough/draft work has been done, cross it through and attach all of them to your answer scripts.

Section A (Answer ALL questions)

(20 marks)

1. A Boolean function of three variables is given by

$$F(X, Y, Z) = (XY + \bar{Z})\,(Y + X\,\bar{Z}).$$

Express F(X, Y, Z) in the **canonical** SOP form (3 marks)

2. The equation for a four variable function is $Y = f(A, B, C, D) = \sum_m (0.2,3,8,10,11,12,14)$.
   a) Draw the truth-table representing the function. (2 marks)
   b) Using the Karnaugh map or otherwise, reduce the function to its minimum two level Sum Of Products (SOP) form. (3 marks)

3. Describe the different kinds of *static hazards* that can occur in combinational logic circuits (2 marks)

4. Draw the logic circuit of a simple 1-to-2 de-multiplexer. (2 marks)

5. In the PLDs, distinguish between ROMs, PALs and PLAs. (2 marks)

6. Using four D type flip flops draw a Serial In Parallel Out (SIPO) shift register. (2 marks)

7. In a Finite State Machine, what is a state transition diagram? (2 marks)

8. Giving the reason state the difference between Moore and Mealy state machines. (2 marks)

Section B (Answer FOUR questions only)

(Each question carries 20 marks)

B1

1. i) a) For the logic circuit shown in Figure B1.a, write down the expression for the output Q. (3 marks)

b) Write down the truth table. (3 marks)

c) The input waveforms at A, B and C are as shown in Figure B1.b. Draw the output waveform

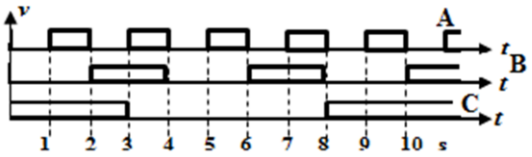

Figure B1.b

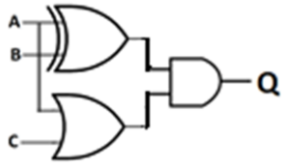

Figure B1.a

(3 marks)

ii) A three variable function Q (A, B, C) as a Karnaugh map is shown in Figure B1.c.

AB / C	00	01	11	10
0	0	1	1	0
1	0	0	1	1

Figure B1.c

a) Reduce the function to its minimum two level products of sum (POS) form (3 marks)

b) Draw the circuit to implement the reduced function. (3 marks)

c) Explain what type of *Hazard* may occur in the circuit? (2 marks)

d) Design and draw the circuit to cover this *Hazard*. (3 marks)

B2. i) It is required to design a circuit that will indicate when the BCD inputs are of even parity.

a) Draw the truth-table representing the function of the circuit. (4 marks)

b) Reduce the function to its minimum two level Sum Of Products (SOP) form. (4 marks)

c) Draw the circuit to implement the function using minimum number of gates. (3 marks)

iii) a) You have been provided with the following two IC chips:

74LS153 – A dual 4-to-1 multiplexer. The internal circuit of the IC is shown in Figure B2.
7401 – A Quad 2 input NOR gate.

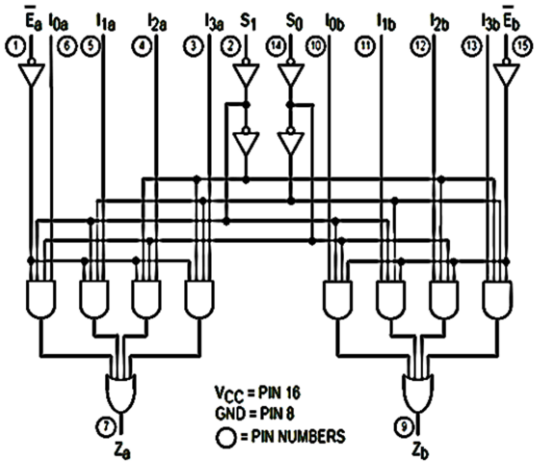

Figure B2: Internal circuit of 74LS153.

State all the connections you will make, including the pin numbers, to extend the IC as an 8-to-1 multiplexer. (6 marks)

b) Explain how the Boolean function $f_{(A,B,C)} = \sum_m(2,6,7)$ can be implemented using this extended multiplexer. (3 marks)

B3. i) $f_{(A, B, C, D, E)} = \sum_m (0,1,8,9,11,15,24,29,30)$ is a 5-variable Boolean function. Using Quine-CcCluskey method or otherwise simplify the function. State the *essential prime implicants* in the function. (12 marks)

ii) a) An 8 × 4 partially programmed PROM is shown in Figure B3. Obtain the simplified expressions for the outputs Y_1 and Y2 (5 marks)

b) How would you program the output line Y_0 so that $Y_0 = BC$? (*Indicate the links in which lines should be blown*) (3 marks)

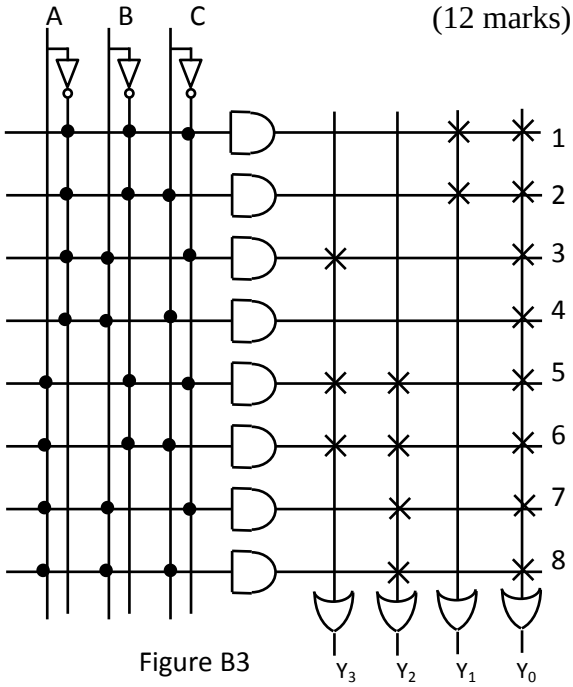

Figure B3

B4. i) a) Stating the reason, determine the number of flip-flops required to construct a decade ripple counter. (3 marks)

b) What is the Boolean expression for an AND gate that will reset the BCD ripple counter. (2 marks)

c) The symbolic representation of a T – type flip flop is shown in Figure B4. Construct the BCD ripple counter using the required number of T – type flip flops and minimum number of gates. Indicate the LSB and MSB. (3 marks)

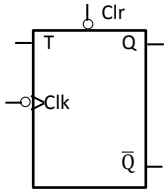

Figure B 4

d) Give the timing diagram of the counter for 12 clock pulses (3 marks)

ii) a) Using **only** three (3) JK flip flops in a counter circuit and a clock of frequency 8.0 kHz, what are the frequencies of the pulses that can be produced? (3 marks)

c) Design a circuit to produce a frequency of 1.6 kHz. Stating the reasons, modify the circuit, using gates, to produce this frequency (6 marks)

B5. i) a) What is meant by '*lock out*' condition in counters. (2 marks)

b) The excitation table for a JK flip flop is shown in Figure B 5.a. Copy and complete the table. (3 marks)

Q_n	Q_{n+1}	J	K
0	0	0	x

Figure 5.a

c) A counter, using 3 JK flip flops, goes through the sequence $4 \rightarrow 6 \rightarrow 7 \rightarrow 3 \rightarrow 1 \rightarrow 4$ …….The unused counts move to the next higher number with the incoming clock pulse. Draw the state diagram for the counter. (2 marks)

d) Figure B 5.b shows the excitation table of the counter circuit. A is for MSB and C for LSB. Copy and complete the table. (8 marks)

Present states			Next states			Flip flop inputs					
A	B	C	A_{+1}	B_{+1}	C_{+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	o	x	1	x

Figure B 5.b

d) Using K –map or otherwise, simplify the input functions J_A and K_A of the MSB flip flop. (5 marks)

THE END