FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

MARKING SCHEME

School : …… **Electrical and Electronic Engineering**……..……..

Course : .....**Engineering Advance Diploma in Electronic & Electrical Eng**

Subject No./ Title : .....**EEE604 – Electro Technology (Electronic)**……..……

Date : …13/06/2014…… , **Examiner** : Mr. **Jiuliasi V. Uluiburotu**….

Model Answers and Marking Scheme
Note: Give a clear indication of answers expected and marks allocated for each part of a question

Section A: [60 marks]

Question 1 Oscillator Design Application

The gain of a certain oscillator system in fig.1 below as a function of frequency is $A(j\omega) = -16 \times 10^6/j\omega$. A feedback path connected around it has $\beta(j\omega) = 10^3/(2 \times 10^3+j\omega)^2$.

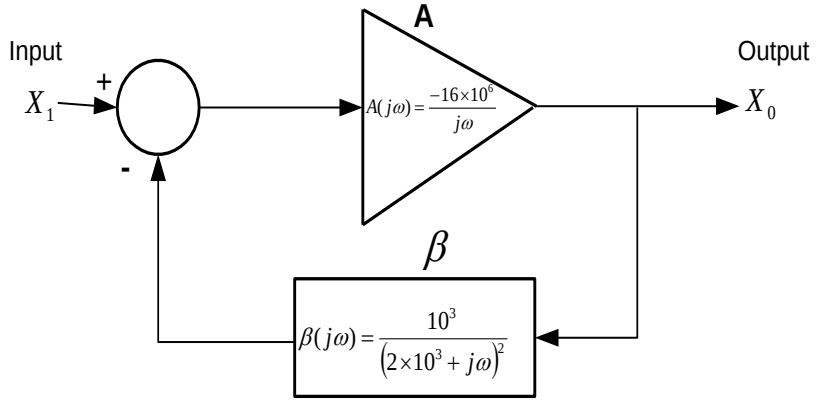


Fig.1 - Oscillator system

Use Rectangular form to determine if the system will oscillate. Determine if your oscillator design will work, what will be the frequency that your oscillator will operate?

The loop gain is

$$A\beta = \left(\frac{-16 \times 10^6}{j\omega}\right)\left[\frac{10^3}{(2 \times 10^3 + j\omega)^2}\right]$$ [1 mark]

$$A\beta = \frac{-16 \text{ x } 10^9}{j\omega(2 \text{ x } 10^3 + j\omega)^2}$$ [1 mark]

To determine if the system will oscillate, we will first determine the frequency, It is important to demonstrate how the same result can be obtained using the *rectangular* form of the criterion: Aβ = 1 + j0.

We first expand the denominator

$$A\beta = \frac{-16\times10^9}{j\omega(2\times10^3 + j\omega)^2}$$ ..... [½ mark]

$$A\beta = \frac{-16\times10^9}{j\omega(4\times10^6 + j4\times10^3\omega^2 - \omega^2)}$$ .....[1½ mark]

$$A\beta = \frac{-16\times10^9}{j\omega[(4\times10^6 - \omega^2) + j4\times10^3\omega^2]}$$ .....[1 mark]

$$A\beta = \frac{16\times10^9}{-4\times10^3\omega^2 + j\omega(4\times10^6 - \omega^2)}$$ .....[2 marks]

To satisfy the Barkhausen criterion, this expression for Aβ must equal 1.
We must therefore set it equal to 1 and simplify equation:

$$1 = \frac{16\times10^9}{-4\times10^3\omega^2 + j\omega(4\times10^6 - \omega^2)}$$ .....[1 mark]

$$4\times10^3\omega^2 - j\omega(4\times10^6 - \omega^2) = 16\times10^9$$ .....[1 mark]

$$\left(4\times10^3\omega^2 - 16\times10^9\right) - j\omega\left(4\times10^6 - \omega^2\right) = 0$$ .....[1 mark]

In order for this expression to equal 0, *both the real and imaginary parts must equal 0.* Setting either part equal to 0 and solving for ω will give us the same result we obtained before:

$$4\times10^3\omega^2 - 16\times10^9 = 0 \Rightarrow \omega = 2\times10^3$$

Determine the value of ω, by using the *real part*.

$$4\times10^3\omega^2 - 16\times10^9 = 0$$ .....[1 mark]

$$4\times10^3\omega^2 = 16\times10^9$$ .....[1 mark]

$$\omega^2 = \frac{16\times10^9}{4\times10^3}$$ ……[1 mark]

$$\omega = \sqrt{\frac{16\times10^9}{4\times10^3}}$$ ……[1 mark]

$$\omega = \sqrt{4\times10^6}$$ ……[1 mark]

$$\underline{\omega = 2\times10^3}$$ ……[1 mark]

either…use 2nd format to determine the value of ω, by using the *imaginary part*.(jω)…..

$$4\times10^6 - \omega^2 = 0 \Rightarrow \omega = 2\times10^3$$ …….[6 marks]

$$4\times10^6 - \omega^2 = 0$$

$$\omega^2 = 4\times10^6$$

$$\omega = \sqrt{4\times10^6}$$

$$\underline{\omega = 2\times10^3}$$

Substituting $\omega = 2 \text{ x } 10^3$, we find

$$|A\beta| = \frac{16 \times 10^9}{2 \times 10^3 (4 \times 10^6 + 4 \times 10^6)} = 1$$ ……....[2marks]

Thus, the Barkhausen criterion is satisfied at $\omega = 2\times10^3$ rad/s and oscillation occurs at that frequency $\left(f = \frac{2 \times 10^3}{2\pi} = 318.3 \text{ Hz}\right)$ ……..…[2marks]

[Q1A. Total - 20 marks]

Question 2 — 2nd Order LP Filter Design

Using the coefficient table attached at the back, design and draw an Active Second Order unity-gain Tschebyscheff Low-pass Filter with a cut-off frequency of 5.5kHz and a 3-dB passband ripple with C1= 22nF.

Look at table-Appendix 2 for coefficients values for a1 and b1 for a 2nd order filter with a1 = 1.0650 and b1 = 1.9305. Specifying C1 as 22nF yields in a C2 of:

$$C_2 = C_1.\frac{4.b_1}{a_1^{\,2}} \qquad \text{(1 mark)}$$

$$C_2 = 22\times10^{-9}.\frac{4\times1.9305}{1.065^2} \qquad \text{(½ mark)}$$

$$C_2 = 149.78\,nF \text{ or } 150nF \qquad \text{(½ mark)}$$

Inserting coefficients a_1 and b_1 into the Resistor equation for R_1 & R_2 results in:

$$R_1 = \frac{a_1.C_2 - \sqrt{(a_1.C_2)^2 - 4b_1.C_1.C_2}}{4\pi f_c C_1.C_2} \qquad \text{(½ mark)}$$

$$R_1 = \frac{1.065\times150nF - \sqrt{(1.065\times150nF)^2 - 4\times1.9305\times22nF\times150nF}}{4\times3.14\times5.5KHz\times22nF\times150nF} \qquad \text{(1 mark)}$$

$$R_1 = \frac{159.75nF - \sqrt{(159.75nF)^2 - 25.48\times10^{-15}}}{227.96\times10^{-12}} \qquad \text{(1½ mark)}$$

$$R_1 = \frac{159.75\times10^{-9}\,F - \sqrt{25.5200625\times10^{-15} - 25.4826\times10^{-15}}}{227.96\times10^{-12}} \qquad \text{(2 marks)}$$

$$R_1 = \frac{159.75\times10^{-9} - 6.120661729\times10^{-9}}{227.96\times10^{-12}} \qquad \text{(2 marks)}$$

$$R_1 = \frac{153.6293383\times10^{-9}}{227.96\times10^{-12}} = 673.93\Omega \qquad \text{(½ mark)}$$

$R_1 = 680\Omega$ preferred value (½ mark)

$$R_2 = \frac{a_1.C_2 + \sqrt{(a_1.C_2)^2 - 4b_1.C_1.C_2}}{4\pi f_c C_1.C_2}$$ (½ mark)

$$R_2 = \frac{1.065\times150nF + \sqrt{(1.065\times150nF)^2 - 4\times1.9305\times22nF\times150nF}}{4\times3.14\times5.5KHz\times22nF\times150nF}$$ (1 mark)

$$R_2 = \frac{159.75nF + \sqrt{(159.75nF)^2 - 25.48\times10^{-15}}}{227.96\times10^{-12}}$$ (1½ mark)

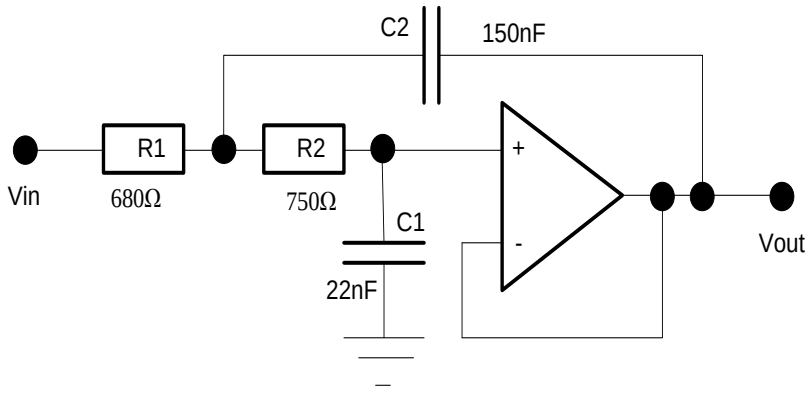
$$R_2 = \frac{159.75\times10^{-9}F + \sqrt{25.5200625\times10^{-15} - 25.4826\times10^{-15}}}{227.96\times10^{-12}}$$ (2 marks)

$$R_2 = \frac{159.75\times10^{-9} + 6.120661729\times10^{-9}}{227.96\times10^{-12}}$$ (2 marks)

$$R_2 = \frac{165.8706617\times10^{-9}}{227.96\times10^{-12}} = 727.63\Omega$$ (½ mark)

$R_2 = 750\Omega$ preferred value (½ mark)

Draw a Low Pass filter circuit and labeled all relevant component with their calculated values.



(2 marks)

Unity Gain Tschebyscheff Low-Pass Filter with 3dB ripple

[Q2A: Total - 20 marks]

Question 3 FET Amplifier Application

An NMOS inverter in the figure -2 below has the following parameters: $V_{T1} = V_{T2} = 2v$. $\beta_1 = 0.35 \times 10^{-3}$, $\beta_2 = 0.035 \times 10^{-3}$ and $V_{DD} = 12v$. Determine the *high* and *low* output voltage.

[20 marks]

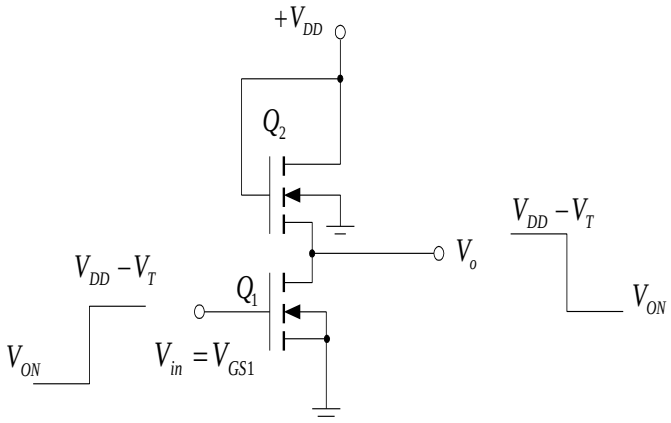


Fig.2 - NMOS Inverter Switch

The high output voltage is $V_{DD} - V_T = 12 - 2 = 10v$. To find the low output voltage V_{ON}, we substitute the parameter values in equation and solve for V_{ON}.

$$\frac{1}{2}\beta_2\left[(V_{DD} - V_{ON}) - V_T\right]^2 = \beta_1\left[(V_{DD} - 2V_T)V_{ON} - 0.5V^2{}_{ON}\right] \text{ .....(½ mark)}$$

$$\frac{1}{2}0.035\times10^{-3}\left[(12v - V_{ON}) - 2\right]^2 = 0.35\times10^{-3}\left[(12v - 4v)V_{ON} - 0.5V^2{}_{ON}\right] \text{ ...(1 mark)}$$

Simplify the equation……cancel the x10^{-3} from both sides.

$$\frac{1}{2}0.035(10 - V_{ON})^2 = 0.35(8V_{ON} - 0.5V^2{}_{ON}) \text{.....(1½ mark)}$$

$$0.0175(10 - V_{ON})(10 - V_{ON}) = 0.35(8V_{ON} - 0.5V^2{}_{ON}) \text{.....(1½ mark)}$$

$$0.0175(V^2{}_{ON} - 20V_{ON} + 100) = 0.35(8V_{ON} - 0.5V^2{}_{ON}) \text{.....(1½ mark)}$$

Further simplify the equation……by get rid of 0.0175 from LHS & take it RHS.

$$\frac{0.0175(V^2{}_{ON} - 20V_{ON} + 100)}{0.0175} = \frac{0.35(8V_{ON} - 0.5V^2{}_{ON})}{0.0175} \text{.....(1½ mark)}$$

Expand the equation by remove the bracket and collect like terms together, leads to the quadratic equation….

$$V^2{}_{ON} - 20V_{ON} + 100 = \frac{0.35\left(8V_{ON} - 0.5V^2{}_{ON}\right)}{0.0175} \quad \text{……..……..….(1½ mark)}$$

$$V^2{}_{ON} - 20V_{ON} + 100 = \left(8V_{ON} - 0.5V^2{}_{ON}\right)20 \quad \text{…….……..……(1½ mark)}$$

$$V^2{}_{ON} - 20V_{ON} + 100 = \left(160V_{ON} - 10V^2{}_{ON}\right) \quad \text{……..…..……..(1 mark)}$$

Simplify and remove the bracket on RHS and shift like terms together from R to L……to form a quadratic equations.

$$V^2{}_{ON} + 10V^2{}_{ON} - 20V_{ON} - 160V_{ON} + 100 = 0 \quad \text{……..…..(1 mark)}$$

$$11V^2{}_{ON} - 180V_{ON} + 100 = 0 \quad \text{……..……(½ mark)}$$

Use the quadratic equation to solve the above…..

$$V_{ON} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \quad \text{……..……(½ mark)}$$

$$V_{ON} = \frac{-(-180) \pm \sqrt{(180)^2 - 4(11)(100)}}{2(11)} \quad \text{…….....(1½ mark)}$$

$$V_{ON} = \frac{180 \pm \sqrt{32400 - 4400}}{22} \quad \text{…….……..….(1 mark)}$$

$$V_{ON} = \frac{180 \pm \sqrt{28000}}{22} \quad \text{……..…...(1 mark)}$$

$$V_{ON} = \frac{180 \pm 167.33}{22} \quad \text{……..……(1 mark)}$$

V_{ON} is either value 1 or value 2…..

$$V_{ON}(High) = \frac{180 + 167.33}{22} = 15.78v \quad \text{or} \quad V_{ON}(Low) = \frac{180 - 167.33}{22} = 0.58v \quad \text{(2 marks)}$$

[Q3A: Total 20 marks]

Section B OPTIONAL – answer any two Question

Question - 1 Series-Fed Class-A Amplifier

Referring to figure 3 below, an input voltage (V_{in}) in a base current of 10mA peak produces the characteristics shown in fig. 3(b) for a series-fed Class A amplifier. Calculate the following:-

(i) Input Power (4 marks)
(ii) Output Power (4 marks)
(iii) Efficiency of Amp (4 marks)
(iv) Power dissipated by the transistor (4 marks)
(v) Identify advantages and disadvantages of negative feedback. (4 marks)

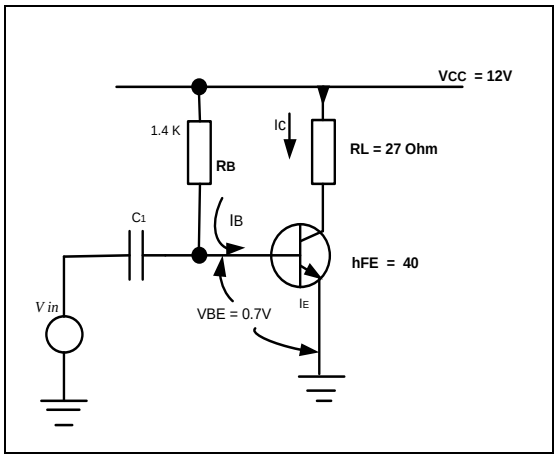


Fig.3a – Series-fed Class A Amplifier

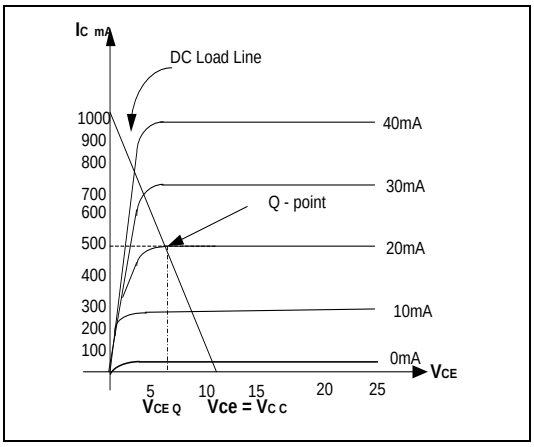


Fig.3b – Series-fed Class A characteristics graph

Q1 - Solution.

(i) To calculate the input power, first calculate I_B to find I_C than find Input power. **[4 marks]**

$$I_B = \frac{Vcc - 0.7}{R_B} = \frac{12 - 0.7}{1.4K\Omega} = 8.07mA \quad \text{(1 mark)}$$

$$I_C = h_{FE}.I_B = 40 \times 8.07mA = 322.8mA \quad \text{(1 mark)}$$

$$Pi_{(DC)} = Vcc \times Ic \quad \text{(½ mark)}$$

$$Pi_{(DC)} = 12 \times 322.8mA \quad \text{(1 mark)}$$

$$Pi_{(DC)} = 3.8736W \quad \text{(½ mark)}$$

(ii) Calculate the Output power, first calculate the peak collector current. **[4 marks]**

$Ic_{(peak)} = h_{FE}.I_B(peak) = 40 \times 10mA = 400mA$ (1 mark)

$Po_{(AC)} = \left(\frac{Ic_{(peak)}}{\sqrt{2}}\right)^2 \times R_L$ (½ mark)

$Po_{(AC)} = \left(\frac{400mA}{\sqrt{2}}\right)^2 \times 27$ (1 mark)

$Po_{(AC)} = 0.08 \times 27$ (1 mark)

$Po_{(AC)} = 2.16W$ (½ mark)

(iii) Calculate the efficiency of the Amplifier. **[4 marks]**

$Efficiency\ \eta = \frac{Po_{(AC)}}{Pi_{(DC)}} \times 100\%$ (2 marks)

$Efficiency\ \eta = \frac{2.16W}{3.8736W} \times 100\% = 55.76\%$ (2 marks)

(iv) Calculation of the power dissipated by transistor as heat. **[4 marks]**

$P_Q = Pi_{(DC)} - Po_{(AC)}$ --- Power dissipated by transistor (½ mark)

$P_Q = 3.8736W - 2.16W$ (2½ mark)

$P_Q = 1.7136W$ (1 mark)

(v) Identify advantages and disadvantages of negative NFB. **[4 marks]**

1. ***Stabilizes an amplifier*** – make gain and operating point independent of device characteristics and temperature.
2. ***Increase the Bandwidth of an amplifier*** – providing useful gain over broader range of frequencies.
3. ***Improve linearity of an amplifier*** – decrease amount of signal distortion.
4. ***Improve noise performance of an amplifier*** – make amplifier quieter.
5. ***Change amplifier impedances*** – raise or lower the input impedances.
6. ***Decrease*** *Current / Voltage Gain*

[Q1B: Total - 20 Marks]

Question 2: Class C Power Amplifier

Fig.4 below shows a class C Power Amplifier with base bias voltage of -5v and V_{CC} = 35v. It is determined that a peak input voltage of 7.6V at 1 MHz is required to drive the transistor to its saturation current of 1.7A

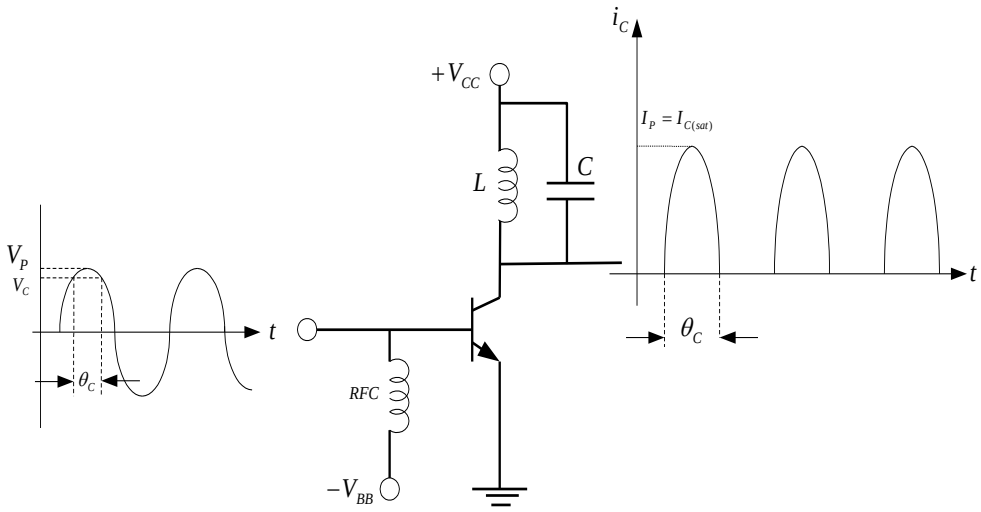


Fig.4 – Class C Power Amplifier

Determine the following:-

(a). Amplifier's conduction angle. (5 marks)
(b). Amplifier's output power at 1MHz. (5 marks)
(c). Amplifier's efficiency. (4 marks)
(d). If the LC tank circuit having C = 270pF is connected in the collector circuit, find the inductance necessary to tune the amplifier. (6 marks)

(a) Calculating the amplifier's conduction angle **[5 marks]**

$$V_C = |V_{BB}| + 0.7$$ (½ mark)

$$V_C = 5v + 0.7 = 5.7v$$ (2 mark)

$$\theta_C = 2\,ar\cos\left(\frac{V_C}{V_P}\right)$$ (½ mark)

$$\theta_C = 2\,ar\cos\left(\frac{5.7}{7.6}\right) = 82.82^0$$ (2 marks)

(b) Calculating the amplifier's output power @ 1MHz **[5 marks]**

$$r_I \approx \left(-3.54 + 4.1\theta_C - 0.0072\theta_C^2\right)\times 10^{-3}$$ (½ mark)

$$r_I \approx \left(-3.54 + 4.1(82.82) - 0.0072(82.82)^2\right)\times 10^{-3}$$ (½ mark)

$$r_I \approx \left(-3.54 + 339.56 - 49.39\right)\times 10^{-3}$$ (1½ mark)

$$r_I = 0.287$$ (½ mark)

$$P_O = \frac{(r_I I_P)V_{CC}}{2} = \frac{(0.287\times 1.7)35}{2} = 8.33W$$ (2 marks)

(c) Calculating the amplifier's efficiency **[4 marks]**

$$r_o = \frac{\theta_c}{\pi(180)}$$ (½ mark)

$$r_o = \frac{82.82}{\pi(180)} = 0.146$$ (1 mark)

$$\eta = \frac{r_1}{2r_O}$$ (½ mark)

$$\eta = \frac{0.287}{2(0.146)} = 0.9828$$ (1 mark)

$$\eta = 0.9828\times 100 = 98.3\%$$ (1 mark)

(d) Calculating the inductance to tuned the amplifier to 1 MHz **[6 marks]**

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$ (½ mark)

$$L = \frac{1}{4\pi^2 {f_O}^2 C}$$ (2 mark)

$$L = \frac{1}{4(3.14)^2\left(1\times 10^6\right)^2\left(270\times 10^{-12}\right)}$$ (1½ mark)

$$L = \frac{1}{10{,}648.368} = 93.91\mu H$$ (2 mark)

[Q2B: Total 20 marks]

Question 3: General Amplifier's Characteristics

(a) Clearly state all advantages and disadvantages of negative feedback.

[3 marks, ½ mark each]

7. ***Stabilizes an amplifier*** – make gain and operating point independent of device characteristics and temperature.
8. ***Increase the Bandwidth of an amplifier*** – providing useful gain over broader range of frequencies.
9. ***Improve linearity of an amplifier*** – decrease amount of signal distortion.
10. ***Improve noise performance of an amplifier*** – make amplifier quieter.
11. ***Change amplifier impedances*** – raise or lower the input impedances.
12. ***Decrease*** *Current / Voltage Gain*

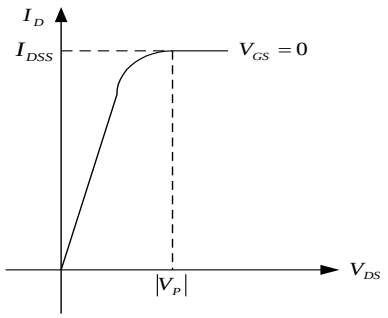
(b) Explain with aid of diagram the effect of increasing V_{DS} in JFET, while gate is shorted to source, $V_{GS} = 0$.

[7 marks]

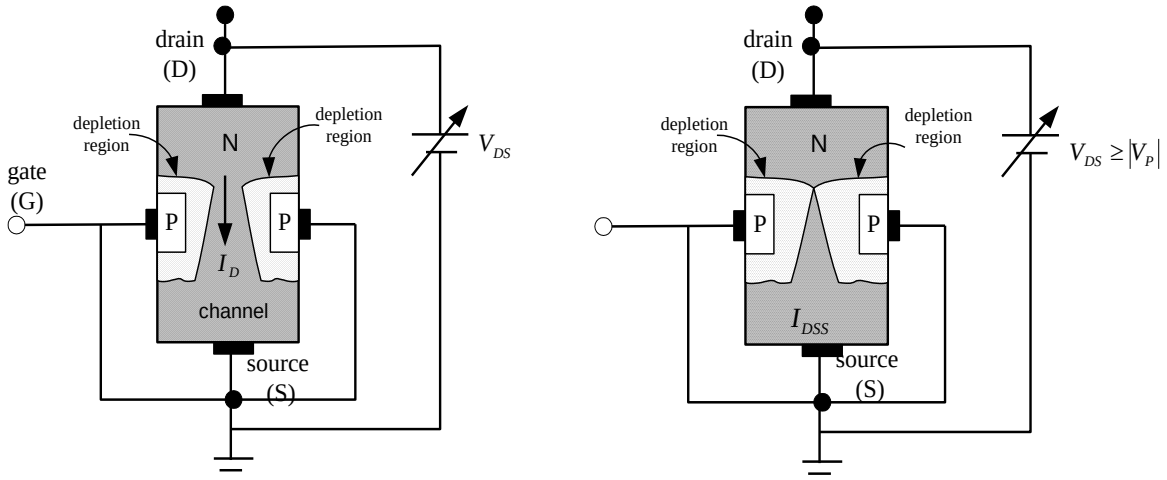
As V_{DS} is increased slightly above 0, we will find that current I_D increases in direct proportion to it. This is due to the fact when voltage is increase across the fixed resistance channel, it also increases the current flowing through it, because of Ohms Law applying here.

As we continue to increase the V_{DS}, we will find a noticeable depletion region begin to form in the channel, as illustrated above in fig.1a & 1b. Note that the depletion region is broader near the Drain end than they are to the Source. This due to the fact that the current flowing channel creates the voltage drop along the length of the channel.

Near the top of the channel, the channel voltage is nearly equal to the V_{DS}, so there is a large reverse-biasing voltage between the N-Channel and the P Gate.



As we proceed down the channel, less voltage is available because of the drop that accumulates through the resistive N-material. Consequently, the reverse-biasing potential between channel and gate becomes smaller and the depletion region becomes narrower as we approach the source.



(c) Find the output voltage of the amplifier shown in figure 3 below, assuming that $r_s = 20\Omega$.

[10 marks]

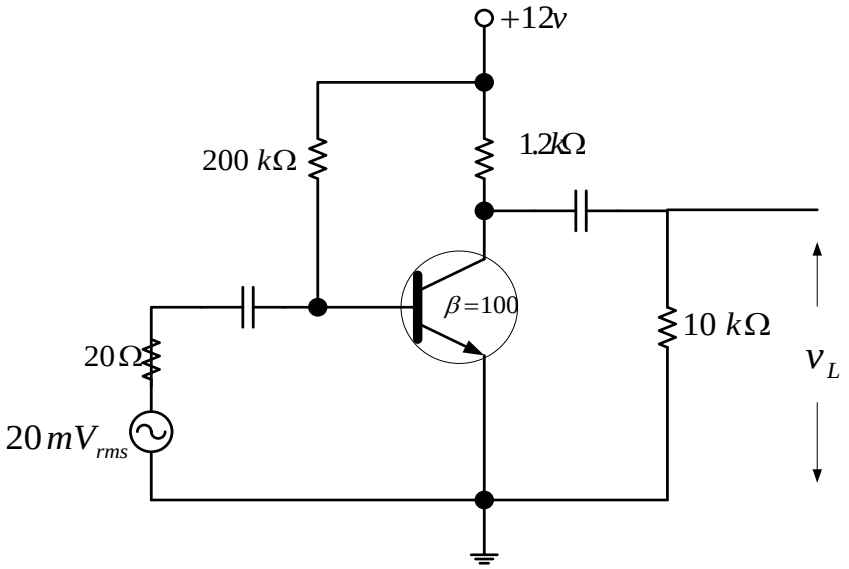


Fig.3 - Common Emitter BJT amplifier

Solution. To find r_e, we must first find the quiescent emitter current [I_e]:

$$I_B = \frac{Vcc - 0.7}{R_B} = \frac{12v - 0.7}{200K\Omega} = 56.5\mu A$$ (1 mark)

$$I_E \approx I_B = \beta I_B$$

$I_E = \beta I_B = 100 \times 56.5\mu A = 5.65mA$ (1 mark)

therefore,

$r_e = \frac{0.026v}{5.65mA} = 4.60\Omega$ (1 mark)

Then calculate the voltage gain,

$A_V = \frac{v_o}{v_{in}} = \frac{-\beta i_b R_C}{\beta r_e i_b} = \frac{-R_C}{r_e}$ (½ mark)

$A_V = \frac{-1.2k\Omega}{4.60\Omega} = -260.87$ (½ mark)

Since $r_S = 20\Omega$, *equation* ……

$\frac{v_L}{v_S} = A_V \left[\frac{R_B \| (\beta r_e)}{r_s + R_B \| (\beta r_e)} \right] \left[\frac{R_L}{R_L + R_C} \right]$ (½ mark)

$\frac{v_L}{v_S} = -260.87 \left[\frac{200k\Omega \| (100 \times 4.60\Omega)}{20 + 200k\Omega \| (100 \times 4.60\Omega)} \right] \left[\frac{10k\Omega}{10k\Omega + 1.2k\Omega} \right]$ (1 mark)

$\frac{v_L}{v_S} = -260.87 \left[\frac{92.0 \times 10^6 / 200.460 \times 10^3}{92.0092 \times 10^6 / 200.48 \times 10^3} \right] \left[\frac{10k\Omega}{11.2k\Omega} \right]$ (1½ mark)

$\frac{v_L}{v_S} = -260.87 \left[\frac{458.94}{458.94} \right] [0.89]$ (1 mark)

$\frac{v_L}{v_S} = -232.17$ (1 mark)

Therefore the magnitude of v_L :-

$v_L = A_V (20mV)$

$v_L = -232.17(20mV) = -4.64V\ rms$ (1 mark)

3B: Total 20 marks]

Question - 4 Digital System Design & OP amps

(a) Figure 6 below shows a 4-bit synchronous shift register with Q_D output connected back to the DA input via an inverter. Assuming the initial state of the register is 0101.

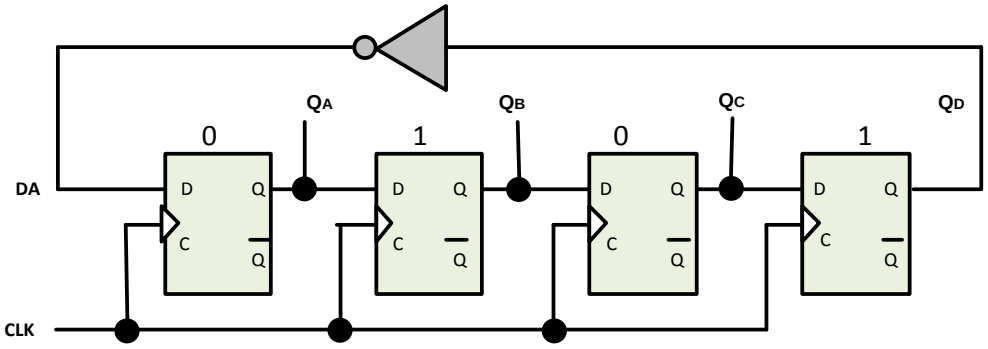


Figure-6: 4-bit Shift Register.

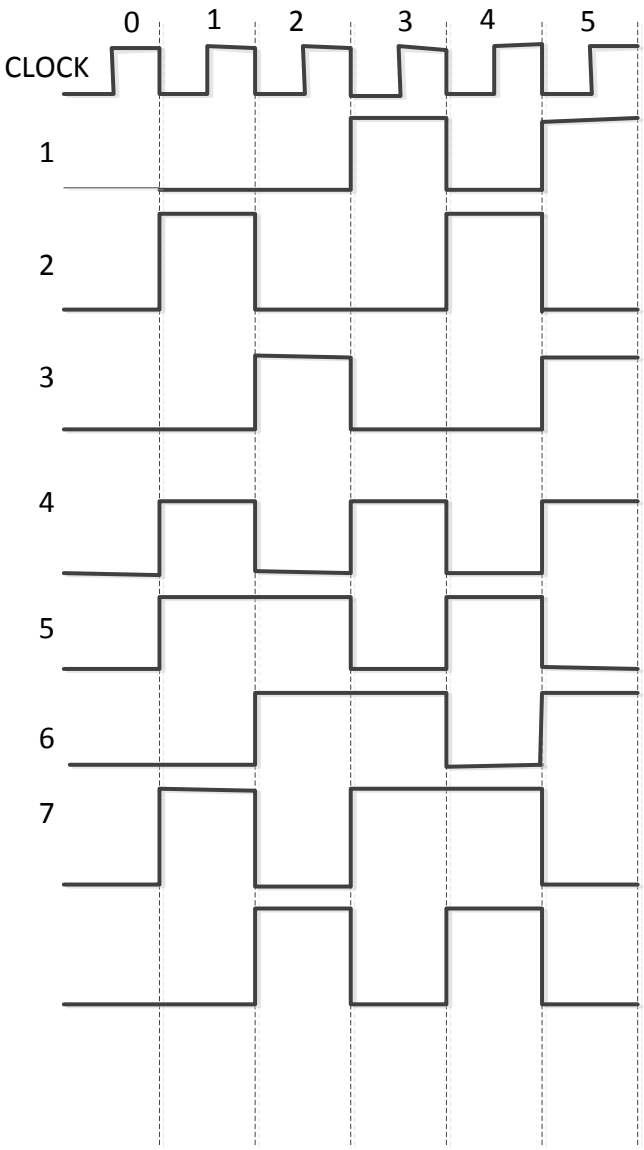
Give a brief account of how the above system works and produce the timing diagram for the output Q_A to Q_D for the next 10 clock pulses, before the output are repeated.

[10 marks]

In the initial state of 0101, the inverted QD output sets DA to be 0. Therefore these are the following sequence:-

a. *first clock pulses shift in a 0 in QA, 0 in QB,1 in QC and 0 in QD.*
b. *the 2nd clk. pulse, produce 1 in QA, 0 in QB, 0 in QC and 1 in QD.*
c. *the 3rd clk. pulse produces 0 in QA, 1 in QB, 0 in QC and 0 in QD.*
d. *the 4th clk. pulse produces 1 in QA, 0 in QB, 1 in QC and 0 in QD.*
e. *the 5th clk. pulse produces 1 in QA, 1 in QB, 0 in QC and 1 in QD.*
f. *the 6th clk. pulse produces,0 in QA, 1 in QB, 1 in QC and 0 in QD.*
g. *the 7th clk. pulse produces 1 in QA, 0 in QB, 1 in QC and 1 in QD.*
h. *the 8th clk. pulse produces 0 in QA, 1 in QB, 0 in QC and 1 in QD.*
i. *After the 8th clk. pulses, the shift register is at its initial state again, so the sequence begins again similar to the 1st clk. pulse.*

(5 *marks)*



(5 *marks*)

(b) In a non-inverting circuit in figure-7 below, the input resistance r_{in} of the op amp on its own is 120kΩ and the voltage gain Av of the Op amp is 220,000. **[6 marks]**

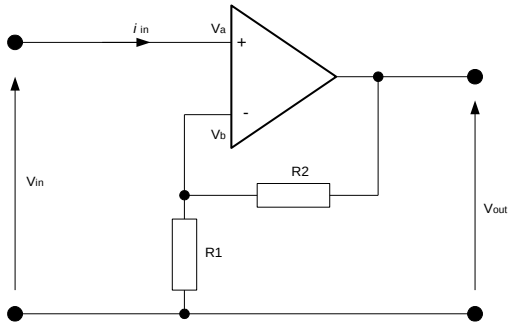


Fig.7 - Non- Inverting Amplifier

Calculate the overall gain G, and the input resistance R_{in} of the circuit above when:-

(i) R_1 = 1KΩ and R_2 = 50KΩ.
(ii) R_2 = 0
(iii) R_1 = 0KΩ and R_2 = 50KΩ

Q 4(c) Solution

(i) $$G = \frac{R_2 + R_1}{R_1} = \frac{50k + 1k}{1k} = 51$$ [½ *mark*]

Input resistance Rin:

$$R_{in} = \frac{A_v R_1}{R_2 + R_1} \times r_{in}$$ [½ mark]

$$R_{in} = \frac{120k\Omega \times 220{,}000 \times 1k\Omega}{50k\Omega + 1k\Omega} = 517.64\ M\Omega$$ [1 *mark*]

[**2 marks**]

(ii) In, when R2 = 0,

$$G = \frac{R_2 + R_1}{R_1} = \frac{0 + 1k\Omega}{1k} = 1$$ [½ *mark*]

Input resistance Rin:

$$R_{in} = \frac{A_v R_1}{R_2 + R_1} \times r_{in}$$ [½ *mark*]

$$R_{in} = \frac{120k\Omega \times 220{,}000 \times 1k\Omega}{0\Omega + 1k\Omega} = 2.64 \times 10^{10}\,\Omega$$ [1 *mark*]

[**2 marks**]

(iii) In, when R1 = 0, R2 = 50k

$$G = \frac{R_2 + R_1}{R_1} = \frac{0 + 50k\Omega}{0k} = 0$$ [½ *mark*]

Input resistance Rin:

$$R_{in} = \frac{A_v R_1}{R_2 + R_1} \times r_{in}$$ [½ *mark*]

$$R_{in} = \frac{120k\Omega \times 220{,}000 \times 0k\Omega}{50k\Omega + 0k\Omega} = 0\,\Omega$$ [1 *mark*]

[**2 marks**]

[6 mark

(c) Briefly explain the advantages & disadvantages of class-D amplifier system. [4 marks]

- *Advantage of Class D amplifiers are:- potential for very high efficiency, approaching 100% due to the fact that semiconductor devices are "on" or "off" in the power stage resulting in low power dissipation in the device as compared to linear amplifier classes.*

- *Disadvantage of Class D amplifiers are:- need for a very good low-pass filter and the fact high speed switching of heavy current generates noise through electromagnetic coupling called electromagnetic interference (EMI).*

[Q4B Total: 20 Marks]

Question - 5 Multiplexer & Registers Design

(a) In the address decoding circuit in figure-8 below for a 4 x 8-bit shift register with an address decoder.

(i) Write down the Truth table for the system.
(ii) Write down the address combination which will select the following register C, A, D, B?
(iii) How many output will the five input decoder have?
(iv) Referring to part (iii), write down the truth table

[10 marks]

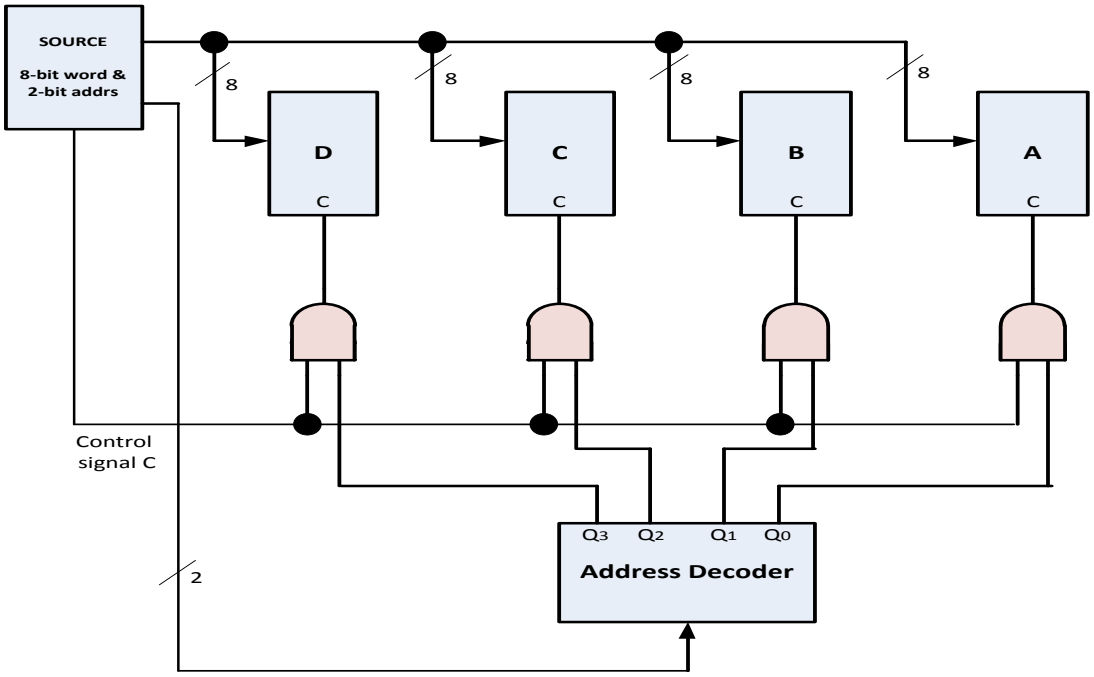


***Figure-8**: 2-Line Address decoder.*

(b) Design and draw a Serial-In Parallel-out Shift Register using D type Flip flop that will do the following:-

(i) Receive the following serial data 100111001 in its input.
(ii) The clock circuit is common, to trigger in its leading edge.
(iii) Draw its Timing Diagram for the next 10 clock pulse.
(iv) Explain the main effect of using Asynchronise clock circuit

[10 marks]

[20 marks]

Q5A - Solution.

(i)

Input			Output			
Cntrl	**A_1**	**A_0**	**Q_3**	**Q_2**	**Q_1**	**Q_0**
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

(*3 marks)*

(ii)

Register C = 1,1,0
Register A = 1,0,0
Register D = 1,1,1
Register B = 1,0,1

(*2 marks)*

(iii)

5 input decoder = 32 output

(*1 mark)*

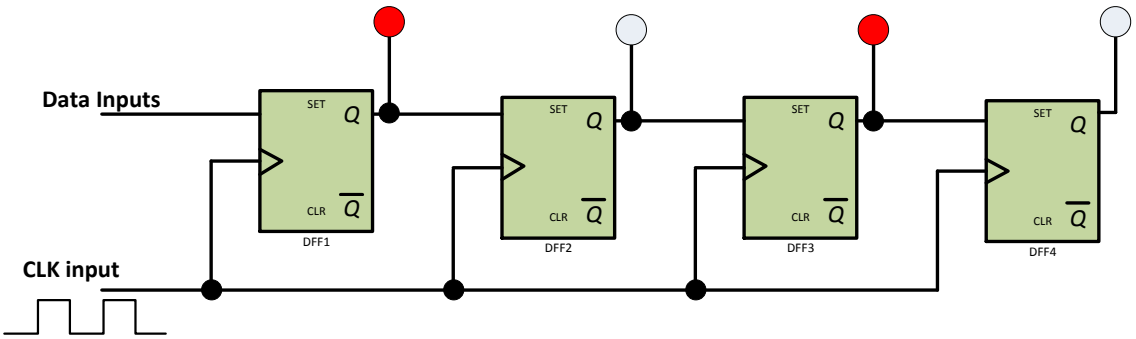
(iv)

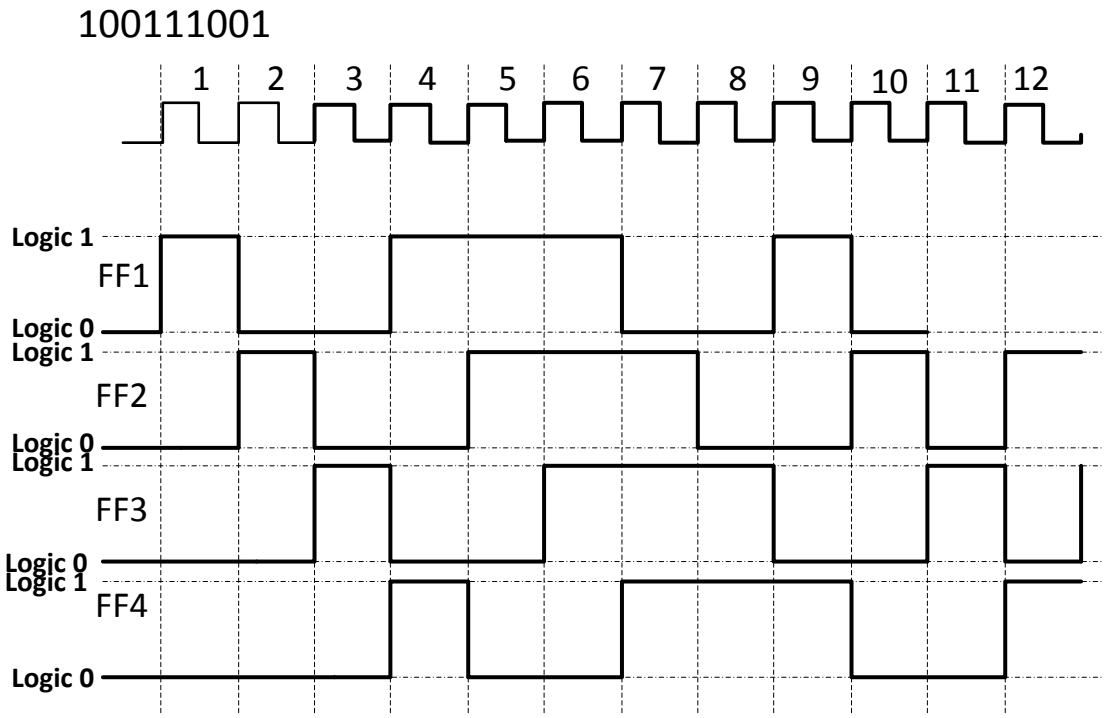
3 input decoder Truth table

Address Input			Selected Output
A2	**A1**	**A0**	
0	0	0	Q_0
0	0	1	Q_1
0	1	0	Q_2
0	1	1	Q_3
1	0	0	Q_4
1	0	1	Q_5
1	1	0	Q_6
1	1	1	Q_7

(*4 marks)*

Q5B - Solution.





The main effect of Asynchronise Clock:-

a) Each flip flop has a separate clock feed.
b) Output displays has a major delay from the 1st to the last FF.

[Q5B: Total 20 marks]

----------THE END ----------