FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE & TECHNOLOGY (CEST)

SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

CERTIFICATE IV IN ELECTRONICS ENGINEERING-STAGE 3

EEE412- DIGITAL ELECTRONICS 1A

FINAL EXAMINATION – PENSTER 1, 2014

DAY/DATE: Wednesday 12/03/2014 TIME:0900AM – 1110AM

SOLUTION

SECTION A MULTIPLE CHOICE 20 MARKS

Question	Solution	Marks
1.	**A**	**1**
2.	**A**	**1**
3.	**B**	**1**
4.	**D**	**1**
5.	**A**	**1**
6.	**A**	**1**
7.	**B**	**1**
8.	**A**	**1**
9.	**A**	**1**
10.	**D**	**1**
11.	**B**	**1**
12.	**D**	**1**
13.	**A**	**1**
14.	**D**	**1**
15.	**C**	**1**
16.	**B**	**1**
17.	**C**	**1**
18.	**A**	**1**
19.	**D**	**1**
20.	**B**	**1**

SECTION B Write True or False (5 marks)

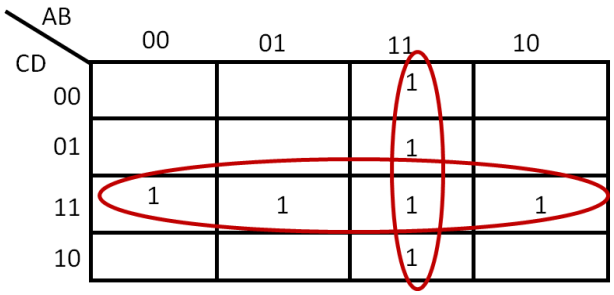
1.	True	**1**
2.	True	**1**
3.	False	**1**
4.	True	**1**
5.	False	**1**

Fill in the blanks (5 marks)

1.	8	**1**
2.	B	**1**
3.	9	**1**
4.	toggle	**1**
5.	hexadecimal	**1**

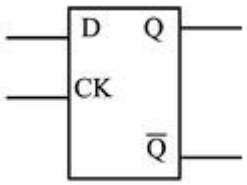
SECTION C (35 marks)

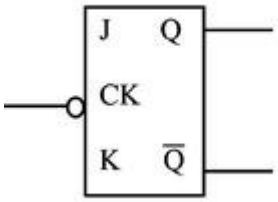
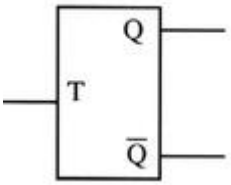
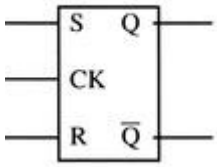
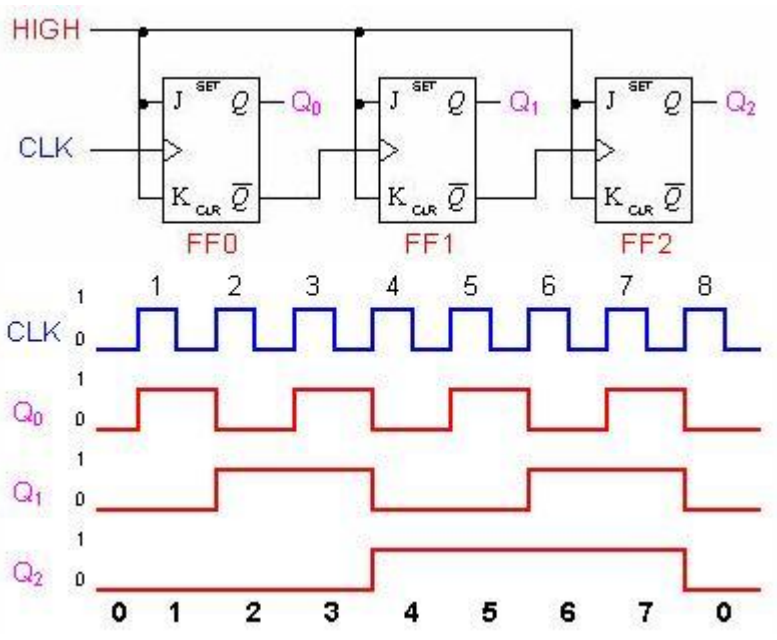
a) i)	NAND gate function	**1**
ii)	OR gate function	**1**
iii)	AND gate function	**1**
b) i)	B B C ↓ ↓ ↓ 11 11 12 $11x16^2$ $11x16^1 + 12x16^0$ 2816 + 176 +12 $= 3004_{10}$	 **0.5** **0.5** **0.5** **0.5**
ii)	445 $4x16^2 + 4x16^1 + 5x16^0$ 1024 + 64 + 5 $=1093_{10}$	 **0.5** **0.5** **1**
c) i)	$F= A(\overline{B} + CD)$	**2**
ii)	$Y= A\overline{B}+ \overline{A}B$	**2**

d)	(A+B).(A+C) = A+B. C AA + AC + BA + BC A + AC + BA + BC A(1+C) + BA + BC A + BA + BC A(1+B) + BC A + BC Therefore L.H.S = R.H.S	**0.5** **0.5** **0.5** **0.5** **0.5** **0.5**
e)	**F = $\bar{A}\bar{B}CD + \bar{A}B\bar{C}D + A\bar{B}\bar{C}D + AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD$**  **F = ABCD** Note: 3 marks is for correct map & 1 mark is for correct expression.	**3** **1**
f) i)	<table><tr><th>A</th><th>B</th><th>C</th><th>Q</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	**4**
ii)	Q= $\bar{A}BC + A\bar{B}C + AB\bar{C}$	**2**
g) i)	Q= $\overline{A+B+C}$ Break the line and change the sign Q= $\bar{A}.\bar{B}.\bar{C}$	**2**

ii)	$P= \overline{\overline{AB} + \overline{\overline{A}\,\overline{B}}}$ $\overline{\overline{AB}} \quad \overline{\overline{\overline{A}\,\overline{B}}}$ $(\overline{\overline{A}} + \overline{B})\ (\overline{\overline{A}} + \overline{\overline{B}})$ $P= (\overline{\overline{A}} + \overline{B})\ (A + B)$	**1** **1** **1**
h)	47 write 47 as binary 101111 add a leading 0 0101111 Exor each pair ANS= **111000**	 **1** **1** **1**
i) i)	821 8+3 2+3 1+3 11 5 4 1011 0101 0100 ANS= 1011 0101 0100	 **0.5** **0.5** **0.5**
ii)	6243 6+3 2+3 4+3 3+3 9 5 7 6 1010 0101 0111 0110 ANS= 1010 0101 0111 0110	 **0.5** **0.5** **0.5**

SECTION D (35 marks)

a) i)		**1**

ii)		**1**
iii)		**1**
iv)		**1**
b)	The clock inputs of all the flip flops are connected together and are triggered by the input pulses.	**2**
c)		**4** **4**

<table>
<tr><td>d) i)</td><td>SR flip flop</td><td>1</td></tr>
<tr><td>ii)</td><td>1</td><td>1</td></tr>
<tr><td>iii)</td><td>Leading edge</td><td>1</td></tr>
<tr><td>iv)</td><td>Counter or shift register</td><td>1</td></tr>
<tr><td>v)</td><td>Negative-edge</td><td>1</td></tr>
<tr><td>e) i)</td><td>0111 1000 0101
7 8 5
ANS= 785_{10}</td><td>2</td></tr>
<tr><td>ii)</td><td>1001 1001 0001 0101
9 9 1 5
ANS= 9915_{10}</td><td>2</td></tr>
<tr><td>f)</td><td><table><tr><td colspan="2">Inputs</td><td colspan="2">Outputs</td><td></td></tr><tr><td>S</td><td>R</td><td>Q</td><td>Q’</td><td>Comments</td></tr><tr><td>0</td><td>0</td><td>Q</td><td>Q’</td><td>No change</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Reset</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Set</td></tr><tr><td>1</td><td>1</td><td>?</td><td>?</td><td>Invalid</td></tr></table>Note: 0.5 mark for each correct entry.</td><td>6</td></tr>
<tr><td>g)</td><td>Ring counter and Johnson counter

1 mark for each correct answer</td><td>2</td></tr>
<tr><td>h)</td><td>A counter has a specified sequence of states, but a shift register does not. A register in general is used for storing and shifting data (1s or 0s) entered into it from an external source. A counter circuit must remember its past states therefore it has to possess memory.</td><td>4</td></tr>
<tr><td></td><td></td><td></td></tr>
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