FNU FIJI NATIONAL UNIVERSITY

COLLEGE: COLLEGE OF ENGINEERING, SCIENCE & TECHNOLOGY (CEST)

SCHOOL: SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING

PROGRAMME: TRADE- DIPLOMA IN ELECTRICAL ENGINERRING - STAGE 3

UNIT CODE: EEE437

TITLE: INTORDUCTION TO ELECTRONICS

ROOM: DATE: TIME: AS PER TIMETABLE

DURATION: 2 HOURS &10 MINS

INSTRUCTIONS TO STUDENTS

1. You are allowed **10 minutes** extra **reading time** during which you are NOT to write.
2. Begin each SECTION on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each attached sheet.
4. Insert all written foolscaps, graph paper, drawing paper, etc. in their correct sequence and secure with a string.
5. For all sheets of paper on which rough/draft work has been done, cross it through and ATTACH these to your answer scripts.
6. Write clearly the number(s) of the question(s) attempted on the top of each sheet.
7. Use of programmable calculator(s) is prohibited.
8. ANSWER ALL QUESTIONS
9. Show all working where necessary.
10. ALWAYS CHECK YOUR WORK BEFORE YOU LEAVE THE EXAM ROOM.

SECTION A DIGITAL ELECTRONICS [50MARKS]

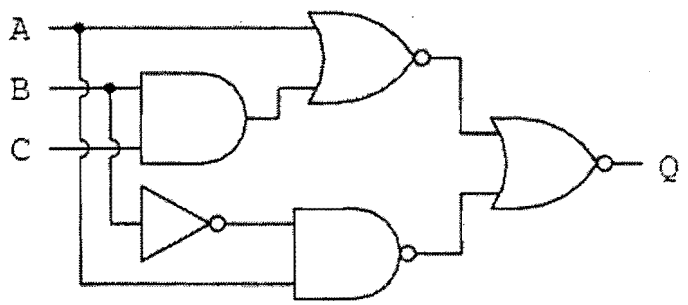
1. Define the following:
   a) Bit **(1 mark)**
   b) Byte **(1 mark)**

2. Convert the following to decimal numbering systems:
   a) 111001_2 **(2 marks)**
   b) 742_8 **(2 marks)**
   c) $1AF_{16}$ **(2 marks)**

3. Convert 0110100000111001 (BCD) to its decimal equivalent. **(1 mark)**

4. Determine the logic gate symbol and the truth table for a two input:
   a) AND gate **(2 marks)**
   b) OR gate **(2 marks)**
   c) NOR gate **(2 marks)**

5. The figure below shows a combinational circuit using universal gates. Determine the output Q and Derive the Boolean equation at the output Q. **(5 marks)**



6. **True/False Questions** **(10 marks)**

State true or false for the following questions in the answer booklet

a) Power dissipation is a measure of a circuit's noise immunity.

b) In a synchronous counter, each state is clocked by the same pulse.

c) Some flip-flops have invalid states.

d) ASCII stands for American Standard Code for Information Interchange.

e) A positive edge-triggered flip-flop changes states with a HIGH to LOW transition on the clock input.

f) A decimal number is converted to BCD by replacing each decimal digit with the appropriate 3-bit binary code.

g) The octal number system consists of eight digits, 0 through to 7.

h) The inverter output is the complement of the input.

i) The hexadecimal number system consists of 16 digits, 0-15.

j) Seven segment is a LED display device.

7. a) Name the input that will set the flip-flop but over-ride the synchronous inputs. **(1 mark)**

b) What are J and K inputs to make the flip-flop avoid the invalid states? **(1 mark)**

c) Which flip-flop has one input beside the clock input? **(1 mark)**

d) Name the flip-flop used in Debounced circuits. **(1 mark)**

e) Registers are storage devices; name the flip-flop that is used for this. **(1 mark)**

f) If the flip-flop is triggered on the 0-1 transition; name the type of clock input. **(1 mark)**

8. Draw the two bit asynchronous counter circuit. **(4 marks)**

9. Draw four cycles clock square waves and show the output timing when is 0-1 triggered. Note that we assume Q_0 and Q_1 are LOW initially **(6 marks)**

10. Draw the block diagrams of the following flip-flops.

a) D-FF **(1 mark)**

b) JK-FF **(1 mark)**

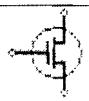
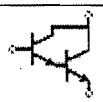
c) T-FF **(1 mark)**

d) SR-FF **(1 mark)**

SECTION B ANALOGUE ELECTRONICS [50MARKS]

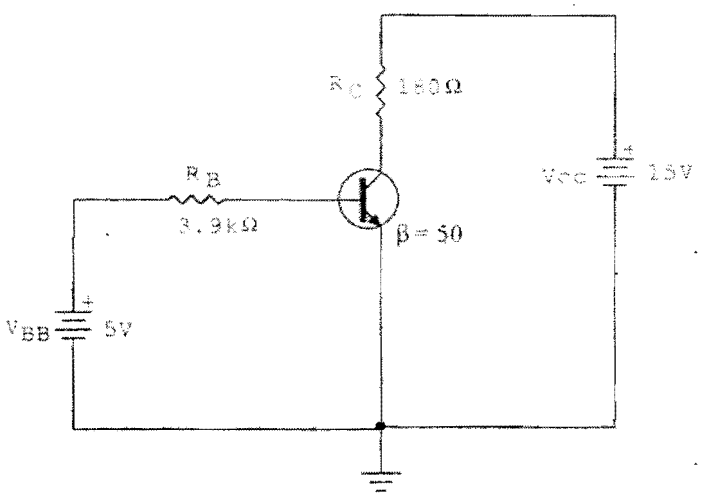
1. **Matching** **(10 Marks)**

Match Column A with Column B in the answer booklet.

COLUMN A		COLUMN B	
1	NPN Bipolar Transistor	A	
2	PNP Bipolar Transistor	B	
3	Darlington Transistor	C	
4	JFET-N Transistor	D	
5	JFET-P Transistor	E	
6	NMOS Transistor	F	
7	PMOS Transistor	G	
8	Ground	H	
9	Speaker	I	
10	OP -Amp	J	

2. List Four (4) Characteristics of an ideal Operational Amplifier: **(4 marks)**

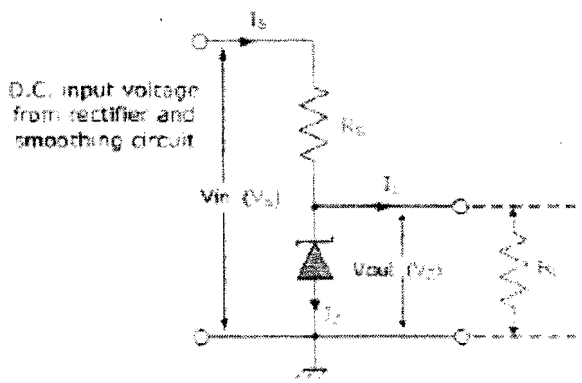
3. A silicon transistor having β=50 is shown below.



Determine the following:

(i)	V_{BE}	**(1 mark)**
(ii)	I_B	**(2 marks)**
(iii)	I_C	**(2 marks)**
(iv)	I_E	**(1 mark)**
(v)	V_{CE}	**(2 marks)**
(vi)	V_{CB}	**(2 marks)**

4. A 5 v stabilised power supply is required from a 12v d.c. input source. The maximum power rating of the Zener diode is 2W as shown below.



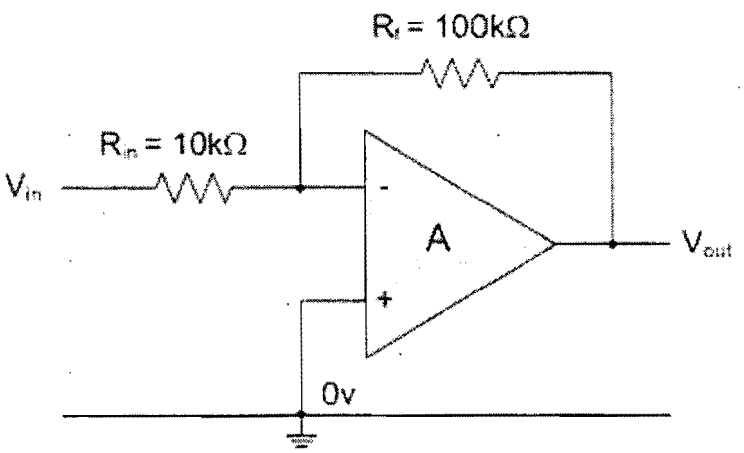
Calculate the following:

i)	The maximum current flowing in the Zener Diode.	**(1 mark)**
ii)	The value of the series resistor, R_S	**(2 marks)**
iii)	The load current I_L if a load resistor of 1kΩ is connected across the Zener diode.	**(1 mark)**
iv)	The total supply current I_S.	**(1 mark)**

5. i) What is heat sink made of? **(1 mark)**
   ii) What is the function of heat sink? **(1 mark)**
   iii) Why are the heat sinks mostly fin shaped? **(1 mark)**

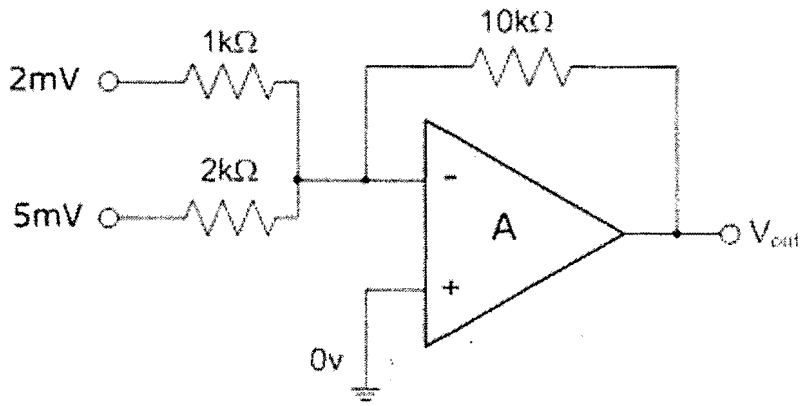
6. Draw the full waveform Bridge rectifier circuit and briefly explain the operation of the circuit and sketch the expected waveforms. **(5marks)**

7. Find the closed loop gain of the following inverting amplifier circuit.



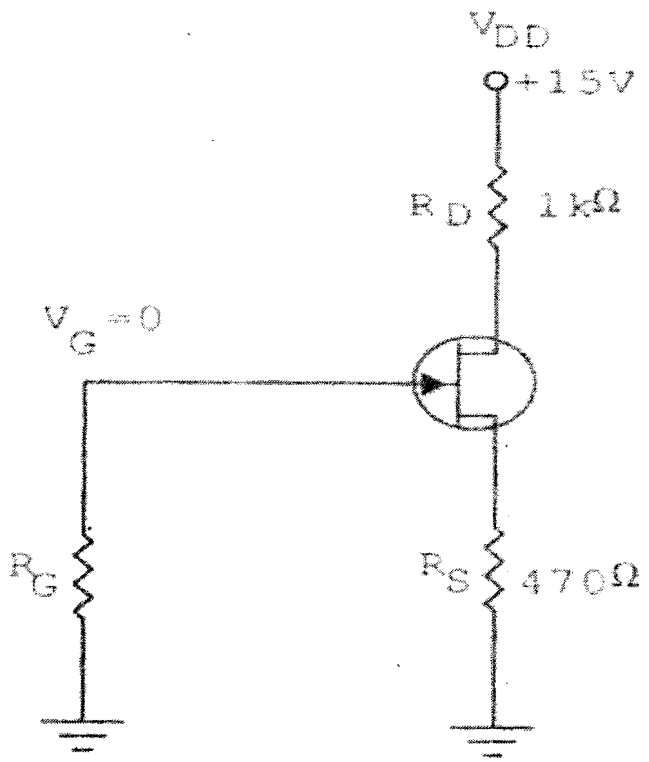
(2 marks)

8. Find the output voltage of the following ***Summing Amplifier*** circuit.



(3 marks)

9. Find V_{DS} and V_{GS} in the figure below, given that I_D=8mA **(4 marks)**



10. Draw the circuit diagram of Basic 5 V DC Power Supply. **(4marks)**

THE END