FNU FIJI NATIONAL UNIVERSITY
College of Engineering, Science & Technology

DIPLOMA IN ELECTRICAL & ELECTRONIC ENGINEERING

EEE434 – DIGITAL ELECTRONICS 2A.

FINAL EXAMINATION - SEMESTER 2 - 2013.

TIME: 2 hours

INSTRUCTIONS TO STUDENTS:

1. You are allowed 10 minutes **EXTRA** as reading time during which you are **NOT** to write.
2. Begin each answer on a fresh page and use both sides of the sheet.
3. Write your candidate number at the top of each attached sheet.
4. Insert all written foolscap, graph paper, drawing paper, etc. in their correct sequence and secure well.
5. For all sheets of paper on which rough/draft work has been done, cross it through and attach to your answer scripts.
6. Show all workings where necessary
7. Diagrams and graphs can be drawn in pencil.
8. Non- programmable calculators are allowed.
9. Attempt all questions ie. Sections A B, C, D & E
10. **Check your work before you leave the room!!**

Section A:

Part 1 MULTIPLE CHOICE **(20 marks)**

Attempt all questions in this section by selecting and writing the correct alphabet beside the number.

1. Which of the following does not represents digital signal data?

   (a) ON and OFF states
   (b) 0 and 1
   (c) 1.5, 3.2, 4.8 and 5V
   (d) 0V and 5V

2. In a binary system, the right-most digit is the

   (a) High significant bit
   (b) Least significant bit
   (c) Most significant bit
   (d) Standard significant bit.

3. Gray code conversion is decided by bit wise operation with

   (a) OR gate
   (b) NOR gate
   (c) XOR gate
   (d) XNOR gate

4. In the NOR gate operation

   (a) Output is HIGH when all inputs are LOW
   (b) Output is Low when all inputs are HIGH
   (c) Output is HIGH when one input is HIGH
   (d) Output is HIGH when one input is LOW

5. In a JK synchronous Flip Flop, if J = 1 and K = 0 then Q will

   (a) Change to 1 if it was on 0
   (b) Toggle
   (c) Remain on 0
   (d) not allowed

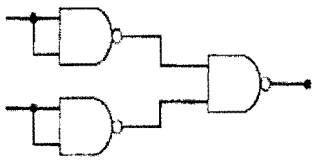
6. What input combination will produce a LOW at the output of a 3-input OR gate?

   (a) When all inputs are LOW
   (b) When any one input is HIGH
   (c) When two inputs are logic 1
   (d) When any one input is LOW

7. The largest decimal number produced in a truth table when using 3 flip flops is:

a) 15
b) 64
c) 32
d) 8

8. The combinational circuit below is equal to



(a) OR gate
(b) XOR gate
(c) AND gate
(d) XNOR gate

9. Using DeMorgans theorem, the expression $\overline{AB+DE}$ is equal to:

(a) $(\bar{A}+\bar{B}+(\bar{D}+\bar{E})$
(b) $(\overline{AB})(\overline{DE})$
(c) (AB).(DE)
(d) Both c and d

10. An asynchronous counter differs from a synchronous counter in:

(a) the number of states in its sequence
(b) the method of clocking
(c) the type of flip flop used
(d) the value of the modulus

11. Which of the following logical operation is represented by the + sign in Boolean algebra?

(a) Inversion
(b) NOR
(c) AND
(d) OR

12. An Exclusive OR gate produces a "1" output when its two inputs are
(a) high
(b) Low
(c) Different
(d) Same

13. A common 7-bit code used to represent numbers, letters, punctuation marks, and control characters is known as:

(a) Hexadecimal
(b) Excess-3 code
(c) ASCII code
(d) Gray code

14. Which of the following will not produce an error code in BCD?

(a) 1011
(b) 0101
(c) 1100
(d) 1010

15. Which segments of a 7-segment display reads decimal 4?

(a) Segments f, g, b, c are lit
(b) Segments a, f, g, c, d are lit
(c) Segments b, c are lit
(d) Segments e, f are lit

16. A four (4) variable Karnaugh map has

(a) 8 cells
(b) 4 cells
(c) 16 cells
(d) 3 cells

17. The binary number 01011 in decimal is

(a) 22
(b) 11
(c) 15
(d) 10

18. An example of a Product Of Sum (POS) expression

(a) A + B(X + Y)
(b) (X+Y) (X+Z)(X+Y+Z)
(c) (AB) +(ZA) +(XY)
(d) Both (a) and (c)

19. Octal to decimal conversion is carried out by:

(a) Finding the sum of product of each digit times its positional value
(b) Converting the binary digits into its 4-bit binary equivalent

(c) Repeatedly dividing the number by 16 and noting the remainder
(d) Converting each digit to its equivalent BCD code.

20. A negative-going transition clock means:

(a) The clock will trigger when it goes from 0 to 1
(b) The clock will trigger when it goes from 1 to 0
(c) The clock will not trigger at all
(d) The clock is positive all the time.

Section B: Number Conversion & Gates (20marks)]

1. Convert the following:

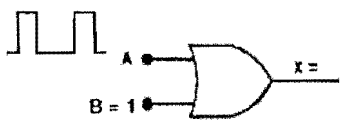
   a) $B2F_{16}$ to decimal (2 marks)
   b) 101101_2 to GRAYCODE (2 marks)
   c) 24.6_8 to Decimal (2marks)
   d) 437_{10} to Binary (2 marks)

2. Use the relevant attached sheet, decode the ASCII code message in a) and encode b):

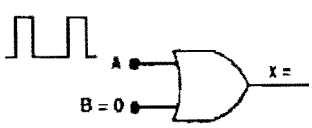
   a) 01001101 01001111 01000011 01000101 01001010 01001111 (2 marks)
   b) TDEEN2A (2 marks)

3. Work out the output x for each gate shown below:

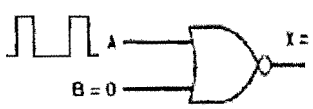
a)



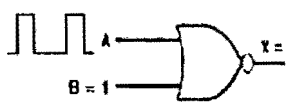
b)



c)



d)



(2 marks each)

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Section C: (20marks)]

1. An electronic motor have 4 input switch A, B, C and D. The motor turns on only under the two condition stated below:
   - Any combination of the input where switches A and B are ON.
   - Any combination of the input where switches A, B and C are OFF

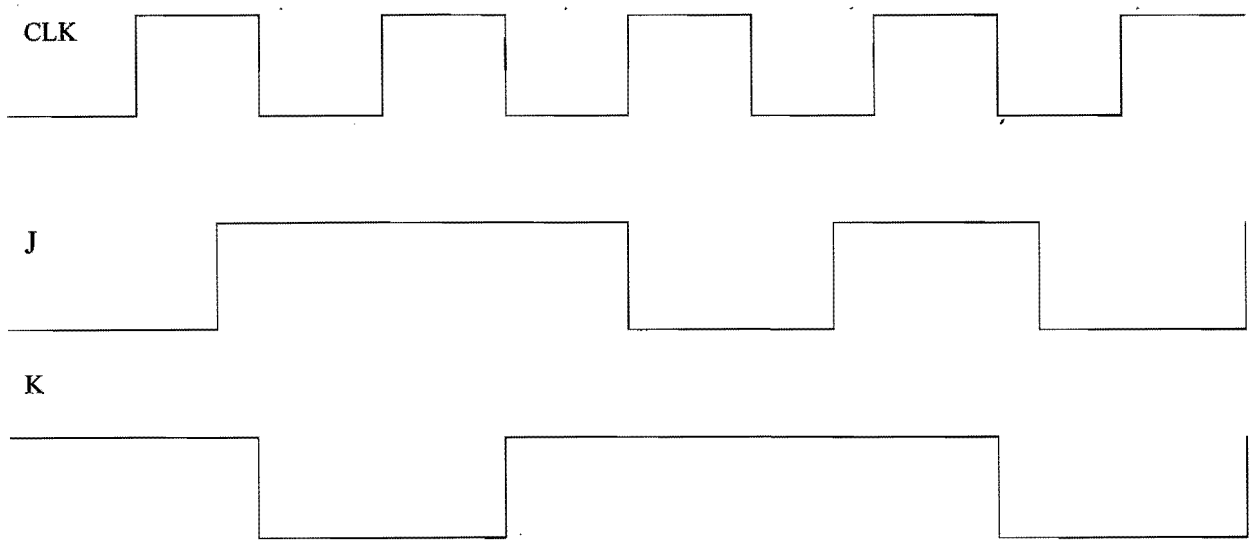
   Compute the following:

   a) Draw the truth table of the four input combinations. (3 marks)
   b) Determine the Boolean expression from the truth table. (3 marks)
   c) Plot the Karnaugh map and prove the simplified Boolean expression. (3 marks)
   d) Determine the SOP expression (3 marks)
   e) Determine the POS expression (3 marks)
   f) Draw the simplified logic circuits (5 marks)

Section D **(20marks)]**

1. Briefly explain the following terms as applied to digital circuits: (8 marks)
   a) Asynchronous
   b) Propagation delay
   c) Fan-out
   d) Noise margin

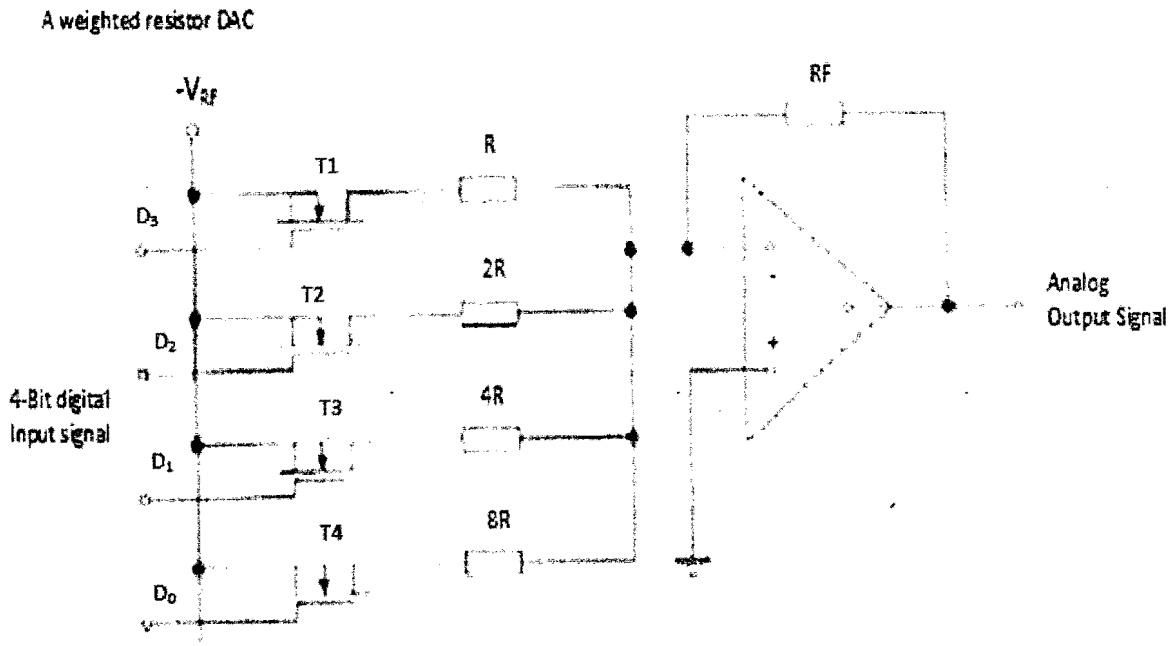
2.
i) Draw a truth table of J K flip flop. (4 marks)
ii) Draw the output Q from the timing diagram below. The Flip Flop is triggered on the negative going transition of the clock. Output Q is initially on logic 1. (8 marks)



Section E **(20marks)**

1. Figure below shows a four-bit Digital to Analog converter. Logic 1 voltage ($-V_{RF}$) is -5 V. Assume RF = 5KΩ and R = 10KΩ.
   Calculate the output voltage (Vout) when the 4-bit digital input word is:

   a) 0101 (4 marks)
   b) 1101 (4 marks)



2. In Boolean algebra, DeMorgan's theorems are simply expressed as follows:
   i) $\overline{A+B} = \overline{A} \cdot \overline{B}$
   ii) $\overline{A.B} = \overline{A} + \overline{B}$

   Draw the logic circuits and truth tables for the above. (8 marks)

3. Simplify the expression $\overline{(\overline{A}+C).(B+\overline{\overline{D}})}$ (4 marks)

----------**THE END**----------

ASCII control characters (character code 0-31)
The first 32 characters in the ASCII-table are unprintable control codes and are used to control peripherals such as printers.

DEC	OCT	HEX	BIN	Symbol	HTML Number	HTML Name	Description
0	000	00	00000000	NUL	&#000;		Null char
1	001	01	00000001	SOH	&#001;		Start of Heading
2	002	02	00000010	STX	&#002;		Start of Text
3	003	03	00000011	ETX	&#003;		End of Text
4	004	04	00000100	EOT	&#004;		End of Transmission
5	005	05	00000101	ENQ	&#005;		Enquiry
6	006	06	00000110	ACK	&#006;		Acknowledgment
7	007	07	00000111	BEL	&#007;		Bell
8	010	08	00001000	BS	&#008;		Back Space
9	011	09	00001001	HT			Horizontal Tab
10	012	0A	00001010	LF
	Line Feed
11	013	0B	00001011	VT	&#011;		Vertical Tab
12	014	0C	00001100	FF			Form Feed
13	015	0D	00001101	CR
	Carriage Return
14	016	0E	00001110	SO	&#014;		Shift Out / X-On
15	017	0F	00001111	SI	&#015;		Shift In / X-Off
16	020	10	00010000	DLE	&#016;		Data Line Escape
17	021	11	00010001	DC1	&#017;		Device Control 1 (oft. XON)
18	022	12	00010010	DC2	&#018;		Device Control 2
19	023	13	00010011	DC3	&#019;		Device Control 3 (oft. XOFF)
20	024	14	00010100	DC4	&#020;		Device Control 4
21	025	15	00010101	NAK	&#021;		Negative Acknowledgement
22	026	16	00010110	SYN	&#022;		Synchronous Idle
23	027	17	00010111	ETB	&#023;		End of Transmit Block
24	030	18	00011000	CAN	&#024;		Cancel
25	031	19	00011001	EM	&#025;		End of Medium
26	032	1A	00011010	SUB	&#026;		Substitute
27	033	1B	00011011	ESC	&#027;		Escape

28	034	1C	00011100	FS	&#028;		File Separator
29	035	1D	00011101	GS	&#029;		Group Separator
30	036	1E	00011110	RS	&#030;		Record Separator
31	037	1F	00011111	US	&#031;		Unit Separator

ASCII printable characters (character code 32-127)
Codes 32-127 are common for all the different variations of the ASCII table, they are called printable characters, represent letters, digits, punctuation marks, and a few miscellaneous symbols. You will find almost every character on your keyboard. Character 127 represents the command DEL.

DEC	HEX	BIN	Symbol	HTML Number	HTML Name	Description
32	20	00100000		&#32;		Space
33	21	00100001	!	&#33;		Exclamation mark
34	22	00100010	"	&#34;	&quot;	Double quotes (or speech marks)
35	23	00100011	#	&#35;		Number
36	24	00100100	$	&#36;		Dollar
37	25	00100101	%	&#37;		Procenttecken
38	26	00100110	&	&#38;	&amp;	Ampersand
39	27	00100111	'	&#39;		Single quote
40	28	00101000	(	&#40;		Open parenthesis (or open bracket)
41	29	00101001	)	&#41;		Close parenthesis (or close bracket)
42	2A	00101010	*	&#42;		Asterisk
43	2B	00101011	+	&#43;		Plus
44	2C	00101100	,	&#44;		Comma
45	2D	00101101	-	&#45;		Hyphen
46	2E	00101110	.	&#46;		Period, dot or full stop
47	2F	00101111	/	&#47;		Slash or divide
48	30	00110000	0	&#48;		Zero
49	31	00110001	1	&#49;		One
50	32	00110010	2	&#50;		Two
51	33	00110011	3	&#51;		Three
52	34	00110100	4	&#52;		Four
53	35	00110101	5	&#53;		Five
54	36	00110110	6	&#54;		Six
55	37	00110111	7	&#55;		Seven
56	38	00111000	8	&#56;		Eight
57	39	00111001	9	&#57;		Nine

58	3A	00111010	:	&#58;		Colon
59	3B	00111011	;	&#59;		Semicolon
60	3C	00111100	<	&#60;	&lt;	Less than (or open angled bracket)
61	3D	00111101	=	&#61;		Equals
62	3E	00111110	>	&#62;	&gt;	Greater than (or close angled bracket)
63	3F	00111111	?	&#63;		Question mark
64	40	01000000	@	&#64;		At symbol
65	41	01000001	A	&#65;		Uppercase A
66	42	01000010	B	&#66;		Uppercase B
67	43	01000011	C	&#67;		Uppercase C
68	44	01000100	D	&#68;		Uppercase D
69	45	01000101	E	&#69;		Uppercase E
70	46	01000110	F	&#70;		Uppercase F
71	47	01000111	G	&#71;		Uppercase G
72	48	01001000	H	&#72;		Uppercase H
73	49	01001001	I	&#73;		Uppercase I
74	4A	01001010	J	&#74;		Uppercase J
75	4B	01001011	K	&#75;		Uppercase K
76	4C	01001100	L	&#76;		Uppercase L
77	4D	01001101	M	&#77;		Uppercase M
78	4E	01001110	N	&#78;		Uppercase N
79	4F	01001111	O	&#79;		Uppercase O
80	50	01010000	P	&#80;		Uppercase P
81	51	01010001	Q	&#81;		Uppercase Q
82	52	01010010	R	&#82;		Uppercase R
83	53	01010011	S	&#83;		Uppercase S
84	54	01010100	T	&#84;		Uppercase T
85	55	01010101	U	&#85;		Uppercase U
86	56	01010110	V	&#86;		Uppercase V
87	57	01010111	W	&#87;		Uppercase W
88	58	01011000	X	&#88;		Uppercase X
89	59	01011001	Y	&#89;		Uppercase Y
90	5A	01011010	Z	&#90;		Uppercase Z
91	5B	01011011	[	&#91;		Opening bracket
92	5C	01011100	\	&#92;		Backslash

93	5D	01011101	]	&#93;		Closing bracket
94	5E	01011110	^	&#94;		Caret - circumflex
95	5F	01011111	_	&#95;		Underscore
96	60	01100000	`	&#96;		Grave accent
97	61	01100001	a	&#97;		Lowercase a
98	62	01100010	b	&#98;		Lowercase b
99	63	01100011	c	&#99;		Lowercase c
100	64	01100100	d	&#100;		Lowercase d
101	65	01100101	e	&#101;		Lowercase e
102	66	01100110	f	&#102;		Lowercase f
103	67	01100111	g	&#103;		Lowercase g
104	68	01101000	h	&#104;		Lowercase h
105	69	01101001	i	&#105;		Lowercase i
106	6A	01101010	j	&#106;		Lowercase j
107	6B	01101011	k	&#107;		Lowercase k
108	6C	01101100	l	&#108;		Lowercase l
109	6D	01101101	m	&#109;		Lowercase m
110	6E	01101110	n	&#110;		Lowercase n
111	6F	01101111	o	&#111;		Lowercase o
112	70	01110000	p	&#112;		Lowercase p
113	71	01110001	q	&#113;		Lowercase q
114	72	01110010	r	&#114;		Lowercase r
115	73	01110011	s	&#115;		Lowercase s
116	74	01110100	t	&#116;		Lowercase t
117	75	01110101	u	&#117;		Lowercase u
118	76	01110110	v	&#118;		Lowercase v
119	77	01110111	w	&#119;		Lowercase w
120	78	01111000	x	&#120;		Lowercase x
121	79	01111001	y	&#121;		Lowercase y
122	7A	01111010	z	&#122;		Lowercase z
123	7B	01111011	{	&#123;		Opening brace
124	7C	01111100	|	&#124;		Vertical bar
125	7D	01111101	}	&#125;		Closing brace
126	7E	01111110	~	&#126;		Equivalency sign - tilde
127	7F	01111111		&#127;		Delete