SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

DIPLOMA IN ELECTRICAL ENGINEERING (ELECTRONICS)

EEE502 DIGITAL ELECTRONICS 2

FINAL EXAMINATION - SEMESTER 1, 2013

MONDAY 03rd June, 2013 1400 – 1610 HOURS VENUE: JAI NARAYAN COLLEGE

INSTRUCTIONS TO CANDIDATES

1. Candidates are reminded that they should have no books, notes, paper or other material in their possession unless their use is specifically permitted by "Instructions to Candidates" set out below.
2. Reading time is of 10 minutes duration.
3. Examination time is of 2 hours duration.
4. There are four (4) questions altogether carrying different marks. Attempt ALL questions.
5. Write your candidate number at the top of each attached sheet.
6. Write the number of the question attempted clearly on the left side of the margin.
10. The examination answer booklet will be collected by the supervisor.
11. The PLA template is on page 6.
12. Datasheets for the TTL Integrated Circuits 74LS47, 74LS138, and 74LS153 are attached at the back.
13. Non-Programmable Calculators may be used.
14. Cell phones are not allowed in the examination venue.

QUESTION 1: LOGIC FAMILIES & ANALOG-TO-DIGITAL CONVERSION

(a) Summarise the comparison of CMOS and TTL logic families under the following characteristics: Power supply; Propagation delay; Power dissipation; Noise immunity. **[4 marks]**

(b) The block diagram of an Analog-to-Digital Converter (ADC) is shown in Figure 1. Explain clearly as to how the analog input V_A is converted to its digital output equivalent. **[1 mark]**

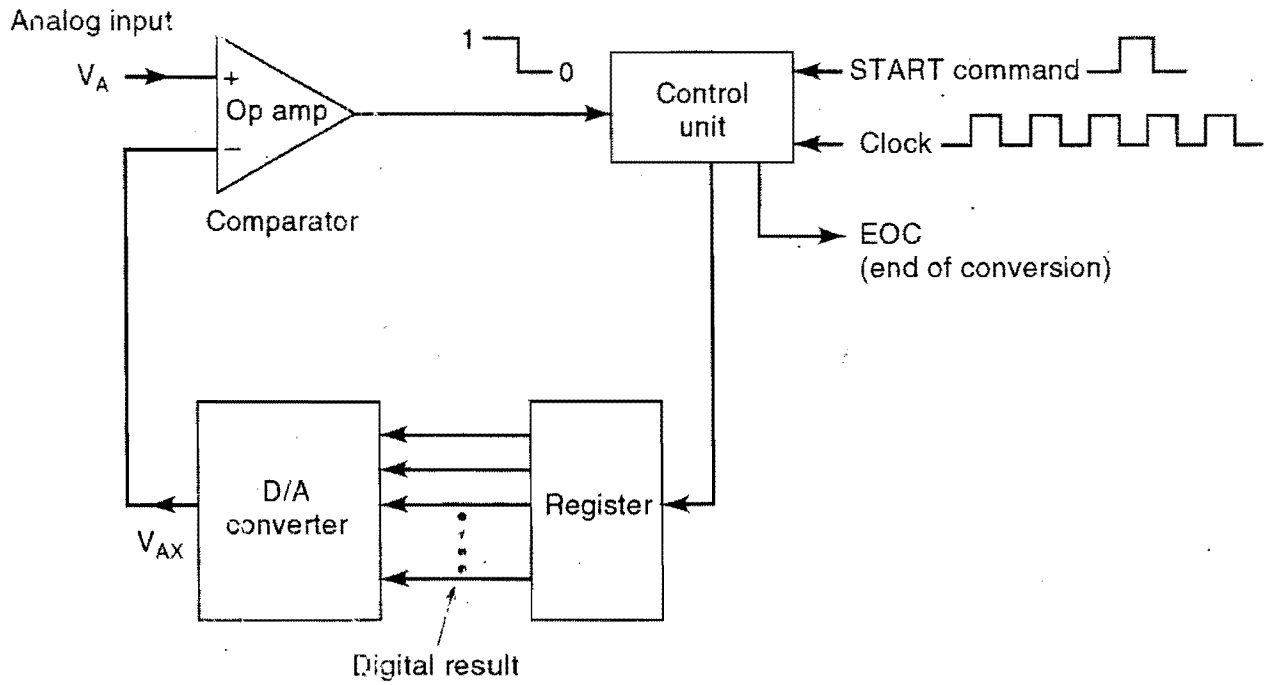


Figure 1: ADC block diagram

[TOTAL = 10 MARKS]

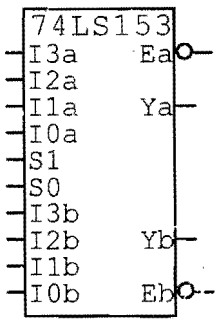
QUESTION 2: LOGIC GATES, DE MORGAN'S THEOREM, MULTIPLEXER, PLA, DECODER

Realize the Boolean functions, $f_1(C,B,A)=\sum_m(0,1,6,7)$ and $f_2=(C,B,A)=\sum_m(1,2,3,5)$ using each of the following procedures:

(a) Utilize NAND gates only **[10 marks]**

(b) Use NOR gates only **[10 marks]**

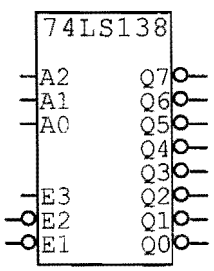
(c) Configure the **74LS153 Dual 4-to-1 Multiplexer** shown. (Datasheet for the 74LS153 is attached at the back). **[10 marks]**



(d) Programmable Logic Array (PLA) with 3 inputs, 3 product terms, and 2 outputs. (Use the PLA Template 1). **[10 marks]**

(f) Utilising the 74LS138 3-to-8 Decoder shown. (The Datasheet for the 74LS138 is attached at the back).

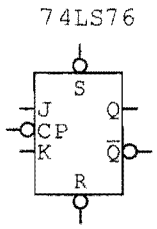
[10 marks]



[TOTAL = 50 MARKS]

QUESTION 3: SYCHRONOUS COUNTER DESIGN – SELF-STARTING

Using the **74LS76 JK flip flop** (shown below), design a Synchronous Modulo 6 Counter that counts in the sequence: 6, 7, 4, 3, 1, 0. The counter is to be made self-starting via suitable connections to the Set and/or Reset pins. Your final product must be a completely functional circuit which utilises the 74LS47 BCD to 7 Segment Decoder/Driver and the display is a Common Anode 7 Segment LED. Break down the solution into the following steps.



(a) Develop the State Transition Diagram. **[4 marks]**

(b) Derive the Circuit Excitation Table. (Hint: Construct the JKFF Excitation Table) **[8 marks]**

(c) Determine the minimised Boolean equation for each J and K input. **[12 marks]**

(d) Implement the self-starting Synchronous Modulo 6 Counter. **[6 marks]**

[TOTAL MARKS = 30 marks]

QUESTION 4: MEMORY MAPPING ADDRESING TECHNIQUES

Consider a RAM integrated circuit with 8 Data Lines, 16 Address lines and 256 Registers with Control signals $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$. The Memory map is from 8900_{16} to $89FF_{16}$.

(a) Determine a plan to efficiently utilize the 16 Address lines. **[5 mark]**

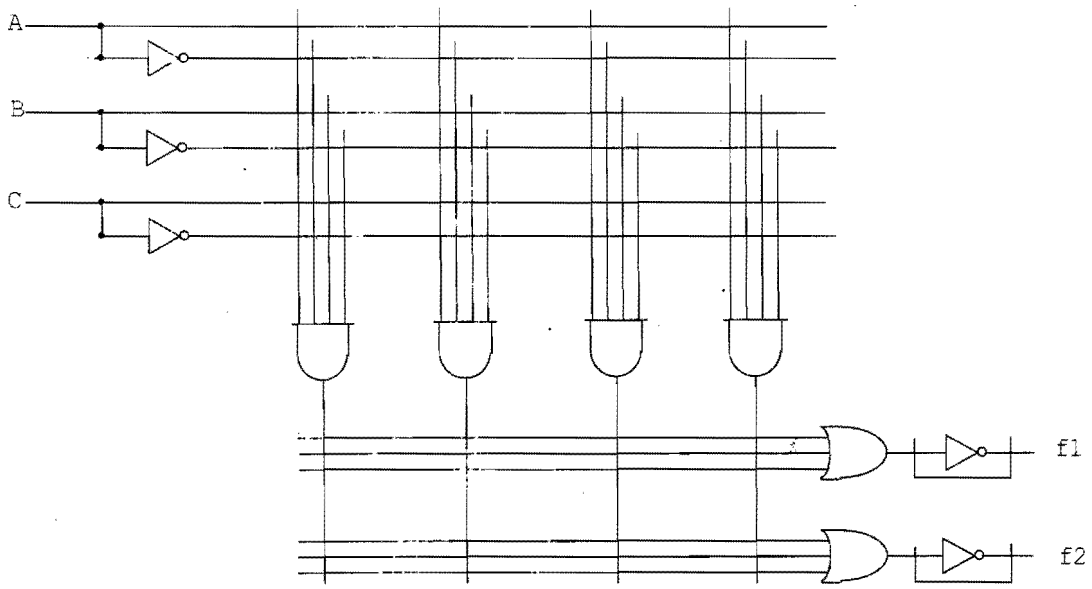
(b) Given the Memory map, derive the hardware components that generate the $\overline{CS}$ signal. **[5 mark]**

[TOTAL = 10 marks]

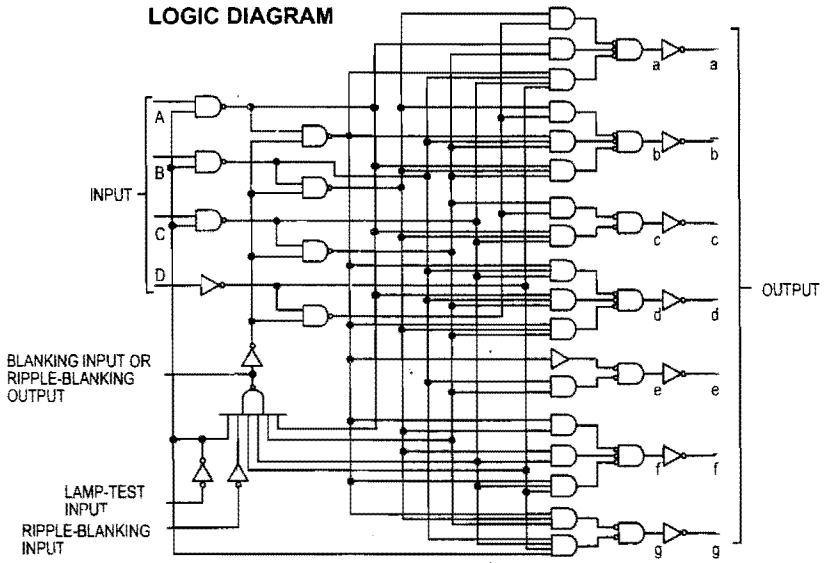
[THE END]

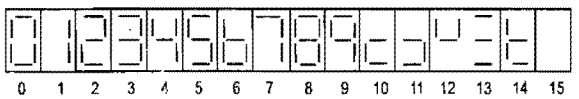
ID No: .....

TEMPLATE 1: PLA Template



LOGIC DIAGRAM





NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:

(A) BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output ($\overline{RBO}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output (BI/$\overline{RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

FUNCTIONAL DESCRIPTION

The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW Outputs ($\overline{O}_0$–$\overline{O}_7$). The LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

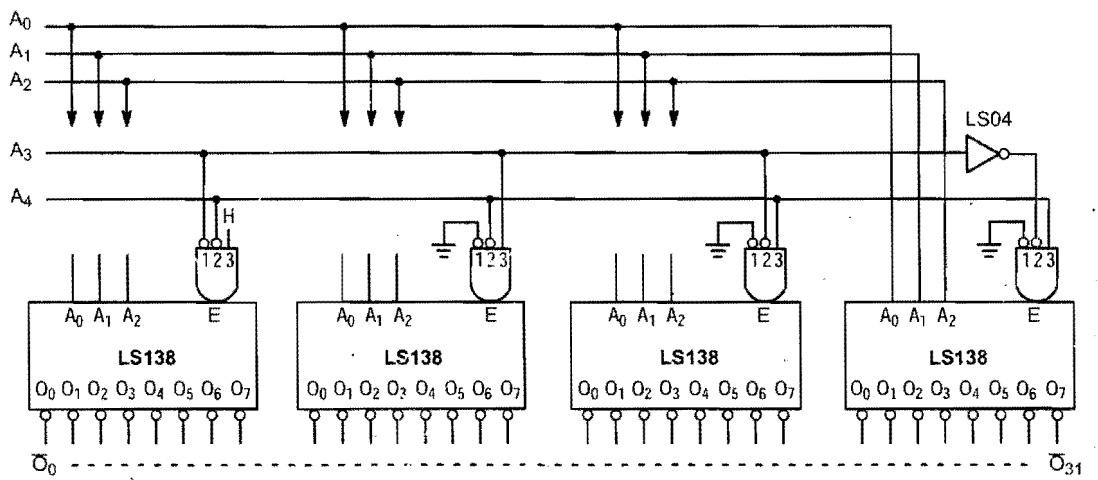


Figure a

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS153
Dual 1-of-4 Line Data Selectors/Multiplexers

General Description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

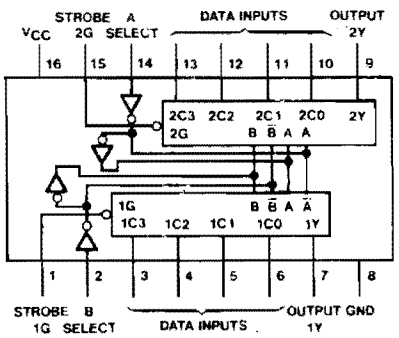
- Permits multiplexing from N lines to 1 line
- Performs at parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low impedance, totem pole outputs
- Typical average propagation delay times
  - From data 14 ns
  - From strobe 19 ns
  - From select 22 ns
- Typical power dissipation 31 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS153M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS153N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = HIGH Level
L = LOW Level
X = Don't Care

