FIJI NATIONAL UNIVERSITY

COLLEGE OF ENGINEERING, SCIENCE AND TECHNOLOGY

School of Electrical & Electronics Engineering

Trade Diploma in Electrical Engineering

EEE437 – Introduction to Electronics

FINAL EXAMINATION

Semester 1, 2012

Date: As per Exam Time Table

Time: As per Exam Time Table (2 hours)

Venue: As per Exam Timetable

Instructions to Students

1. You are allowed an extra ten (10) minutes of reading time during which you are NOT allowed to write.
2. Attempt ALL questions in this examination booklet
3. Write your answers in the answer booklet provided.
4. Write your Student ID number on each page used.
5. Begin each Section on a fresh page and use both sides of the answer sheet.
6. You may use calculators provided they are non-programmable.
7. Clearly number the questions in your answer paper in their correct sequence and write legibly. Show all working.
8. Attach any extra sheets used to your answer booklet securely with the string provided.

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Section A: Multiple Choices [12 marks]
Choose the letter of the BEST choice.

1. The product of multiplying the binary numbers 1001 by 011 is:

   a) 11001
   b) 11011
   c) 11100
   d) 01101

2. The largest decimal number that can be produced when using 6 bits is:

   a) 15
   b) 32
   c) 63
   d) 31

3. The ASCII code is:

   a) a positional value code
   b) a minimum change code
   c) a straight binary code
   d) an alphanumerical code

4. An Asynchronous counter differs from a synchronous counter in:

   a) the number of states in its sequence
   b) the method of clocking
   c) the types of flip-flops used
   d) the value of the modulus

5. An 8-bit DAC has a resolution of:

   a) 0.1000%
   b) 0.0244%
   c) 0.3920%
   d) 1.0000%

6. In an R/2R DAC, there are:

   a) four values of resistors
   b) two resistor values
   c) one resistor value
   d) a number of resistor values equal to the number of inputs

7. A Flash ADC uses:

   a) op-amps
   b) counter
   c) an integrator
   d) flip-flops

8. In a binary weighted DAC, the resistors on the inputs:

   a) determine the amplitude of the analog signal
   b) determine the weights of the digital inputs
   c) limit the power consumption
   d) prevent loading on the source

9. When the frequency of the input signal to a CMOS gate is increased, the average power dissipation:

   a) decreases
   b) increases
   c) does not change
   d) decreases exponentially

10. Proper handling of CMOS device is necessary because of its:

    a) fragile construction
    b) high-noise immunity
    c) susceptibility to electrostatic discharge
    d) smaller power dissipation

11. In a npn transistor, the p regions are:

    a) base and emitter
    b) base and collector
    c) collector and emitter
    d) only base

12. FET is a _____ controlled devise.

    a) voltage
    b) current
    c) power
    d) none of the above

Section B: Digital Electronics [58 marks]

Question 1: Number Systems [18 marks]

a) An even parity system receives the following code groups: 10110, 11010, 110011, 110101110, and 1100010101010. Determine which groups, if any, are in error. [1 mark]

b) Convert 315_4 to its decimal equivalent. [2 marks]

c) Represent the decimal number 81.375 in:

i) Binary [3 marks]

ii) Octal [2 marks]

d) Convert the decimal number -21 to its equivalent hexadecimal number [3 marks]

e) Determine the decimal value of the single precision floating-point binary number:
1 10011000 10000100010100110000000 [4 marks]

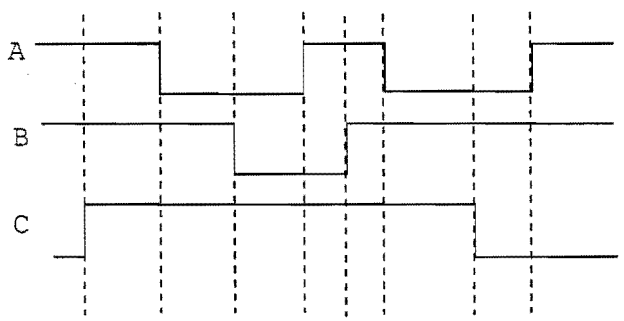
f) Add the following BCD number 00010110 to 00010101. [3 marks]

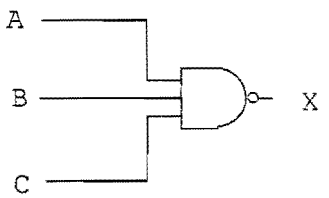
Question 2: Combinational Logic Functions and Gates [20 marks]

a) Electronics can be divided into two broad categories, digital and analog. With aid of diagrams, explain the difference between these two quantities. [3 marks]

b) Using Boolean algebra techniques and DeMorgan's theorems, simplify the expression
$\overline{\overline{A}+\overline{B}}+A(\overline{\overline{BC}})+B(B+C)$ [4 marks]

c) Show the output waveform for the three input gate shown below with its proper time relationship to the inputs. [4 marks]





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d) A function F is given to be $F = \overline{A}B + AB\overline{C} + A\overline{B}C$.

i) Show the truth table for this function (show all working). [3 marks]

ii) Determine the standard POS expression. [2 marks]

iii) Determine the minimum SOP expression using Karnaugh map. [2 marks]

iv) Implement the circuit diagram from the minimized expression in part (iii). [2 marks]

Question 3: Logic Families, Flip-Flops, and ADC & DAC [20 marks]

a) There are two types of seven segment displays. Name the type that requires a HIGH at the input to activate (turn on/light) a particular segment. [1 mark]

b) Using the information on noise margins given below, which family of devices, 5V CMOS or TTL would you recommend to be used in a low-noise environment. [1 mark]

For 5V CMOS: $V_{NH} = 0.9$ V, $V_{NL} = 1.17$ V

For 5V TTL: $V_{NH} = 0.40$ V, $V_{NL} = 0.40$ V

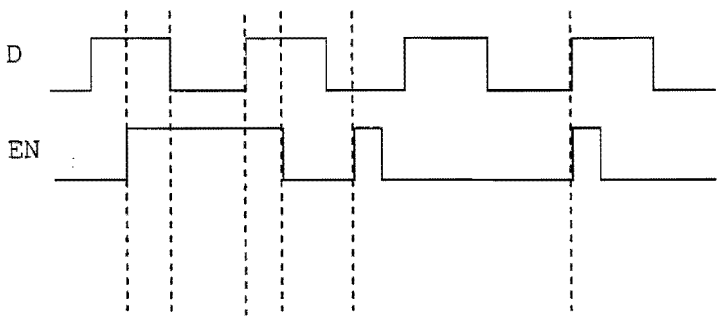
c) List two characteristics that made TTL superior compared to CMOS in the past. [2 marks]

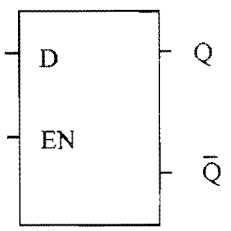
d) Which type of ADC is commonly used in digital voltmeters and other types of measurement instrument? [1 mark]

e) State the most widely used method of Analog-to-Digital converter. [1 mark]

f) State one of the disadvantages of Binary-Weighted-Input DAC. [1 mark]

g) Determine the output (Q) waveform for the gated D latch with proper time relationship to the inputs as shown below. [2 marks]





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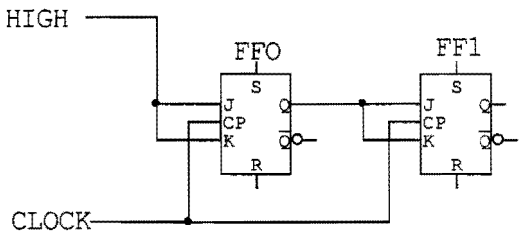
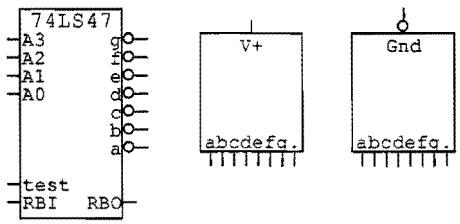
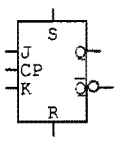
h) Show how the 2-bit synchronous binary counter given below can be modified to obtain a 3-bit binary counter. [3 marks]



i) Given the following components, show how you will connect these to your 3-bit synchronous counter circuit in part (h) to display the decimal value of binary output. Use a block diagram to represent your circuit in part (h). Select the correct 7 segment display to be used from the two given. [2 marks]



j) Show how an asynchronous counter can be implemented having a binary sequence from 000 to 101 (recycles between these two binary numbers) using JK flip-flops and logic gates. Use the block diagram of the CMOS JK flip-flop given below. [6 marks]

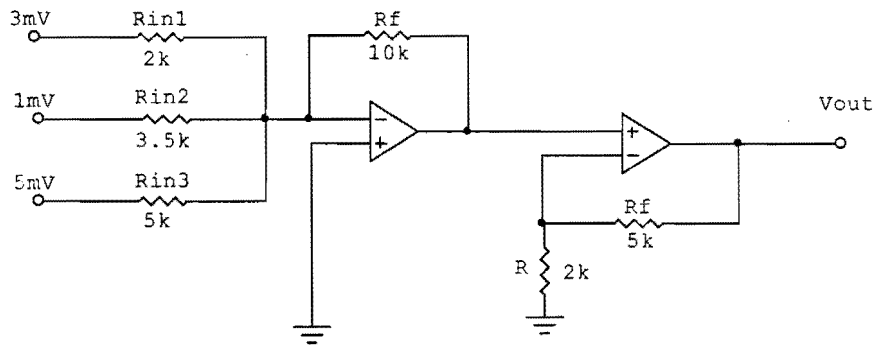


Section C: Analog Electronics [30 marks]

Question 1: Amplifier Principles [7 marks]

a) State four characteristics of an ideal op-amp. [2 marks]

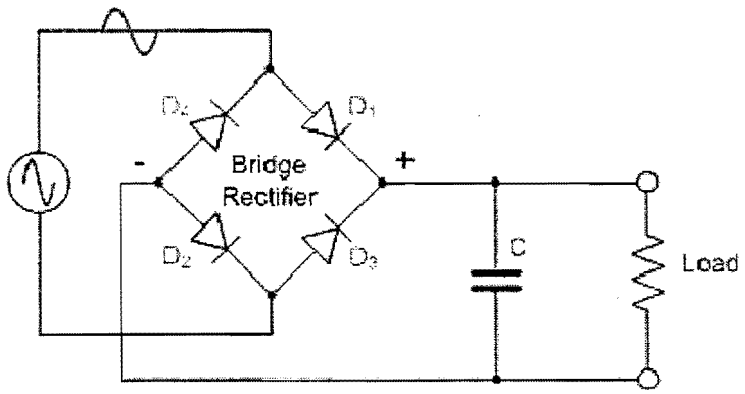
b) Find the output voltage for the following circuit. [5 marks]



Question 2: Rectifiers and Simple Power Supplies [12 marks]

a) With the aid of diagrams, briefly explain what happens to the depletion layer in a pn junction when it is forward biased. [2 marks]

b) Refer to the circuit given below of a full wave bridge rectifier to answer the following questions.



i) State the special name of the capacitor, C. [1 mark]

ii) Clearly indicate the direction of flow of current for the positive half cycle on the circuit provided in the solution sheet. [2 marks]

iii) Draw a clearly labeled output waveform for the circuit. [2 marks]

Please Turn Over

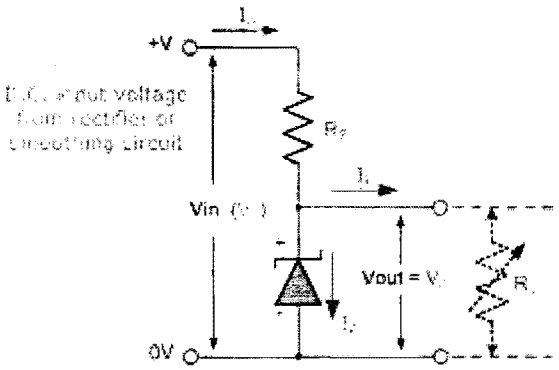
c) A 6 V stabilized power supply is required from a 12 V dc input source. The maximum power rating of the Zener diode is 2.6 W. Using the circuit given below, calculate:

i) the maximum current flowing in the Zener diode [1 mark]

ii) the value of the series resistor, R_s. [1 mark]

iii) the total supply current, I_s when connected to a load of 1 kΩ. [2 marks]

iv) What is the special name given to the series resistor? [1 mark]

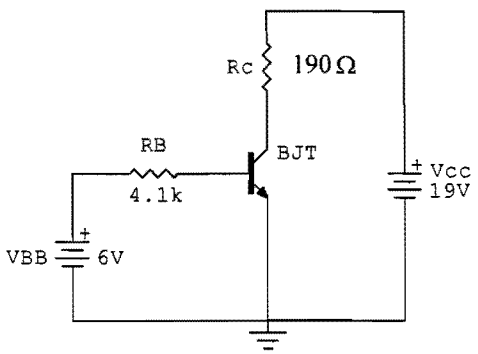


Question 3: Discrete Amplifying Devices [11 marks]

a) Draw the symbol of a P-channel JFET. [1 mark]

b) Draw a typical mutual characteristics curve for an N-channel JFET operating in common source mode. [2 marks]

c) A silicon transistor having α = 0.986 is shown below:



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Determine the following:

i) V_{BE} [0.5 mark]
ii) I_B [1 marks]
iii) I_C [2 marks]
iv) I_E [1.5 marks]
v) V_{CE} [1.5 marks]
vi) V_{CB} [1.5 marks]

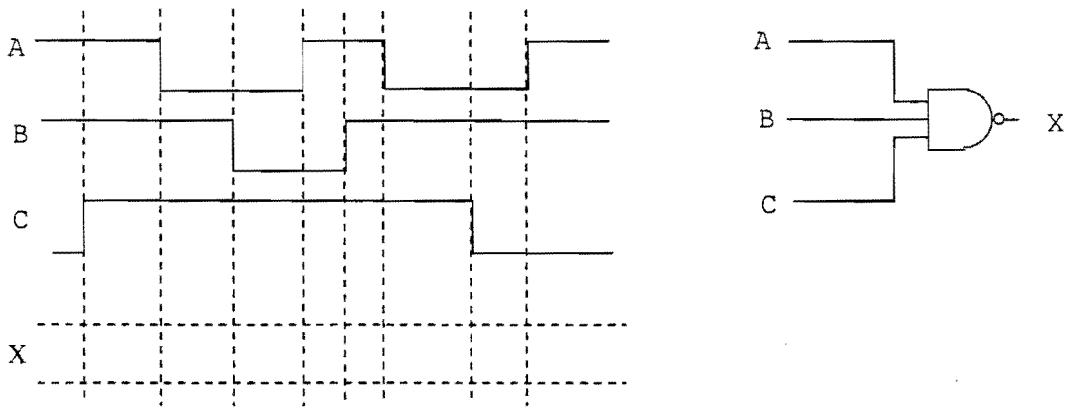
THE END

Please find attached the solution sheet for Section B; Q2(c) and Q3 (g) and Section C; Q2 (b) (ii) on the next page. Attach this to your answer booklet.

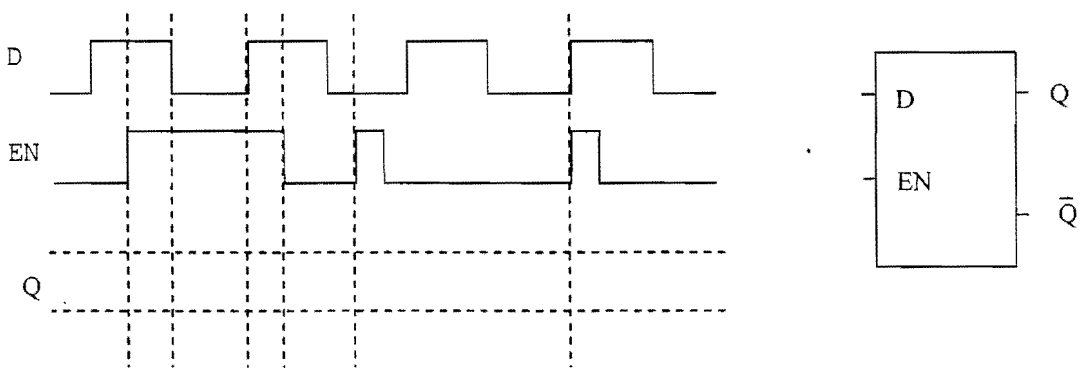
ALL THE BEST FOR THE EXAMINATION

SOLUTION SHEET (Please attach this sheet to your Answer Booklet)

Section B: Question 2 (c)



Section B: Question 3 (g)



Section C: Question 2 (b)

(iii)